- [23] H.T. Vergos, C. Efstathiou, and D. Nikolos, "Diminished-One Modulo 2ⁿ+1Adder Design," IEEE Trans. Computers, vol. 51, no. 12, pp. 1389-1399, Dec. 2002.
- [24] C. Efstathiou, H.T. Vergos, and D. Nikolos, "Modulo 2n -1 Adder Design Using Select Prefix Blocks," IEEE Trans. Computers, vol. 52, no. 11, pp. 1399-1406, Nov. 2003.
- [25] H.T. Vergos and C. Efstathiou, "Efficient Modulo 2ⁿ+1Adder Architectures," Integration, the VLSI J., vol. 42, no. 2, pp. 149-157, Feb. 2009.
- [26] G. Dimitrakopoulos and D. Nikolos, "High-Speed Parallel-Prefix VLSI Ling Adders," IEEE Trans. Computers, vol. 54, no. 2, pp. 225-231, Feb. 2005.
- [27] Rakhi Thakur and Kavita Khare "High Speed FPGA Implementation of FIR Filter for DSP Applications",International Journal of Modeling and Optimization, Vol. 3, No. 1, February 2013