An Investigation of a Double-Tail Comparator for Low-Power Applications

N. Sindhu and M. Archana

Abstract--- Many high-speed analog to digital converters, such as flash ADCs, require high-speed, low power comparators with small chip area. CMOS dynamic comparator with dual input, dual output inverter stage is suitable for high speed analog-to-digital converters with low voltage and low power. A single tail comparator is replaced with a double tail dynamic comparator which reduces the power and voltage by increasing the speed. The proposed Dynamic comparator is a modified version of a low voltage low power double tail comparator for area efficient and double edge triggered operation. The simulated data presented is obtained using TANNER EDA tool with 130 nm technology. In the proposed dynamic comparator, both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 5GHz at supply voltage of 1.8V.

Keywords--- Double-tail Comparator, Dynamic Latch Comparator, High Speed Analog-to-digital Converters (ADCs), Low-power Analog Design

I. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog to digital converters (ADCs). High speed flash ADCs, require high speed, low power and small chip area. Comparators are known as 1-bit analog to digital converter and hence they are mostly used in large abundance in A/D converter.

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A comparator is same as that like of an operational amplifier in which they have two inputs (inverting and non-inverting) and an output. The function of a CMOS comparator is to compare an input signal with a reference signal which produces a binary output signal. Comparator uses back-to-back cross-coupled inverters to convert a small input voltage-difference to digital output in a short period of time.

It is more challenging to design a high speed comparator with a small supply voltage [1]. The performance of the comparator plays an important role in realization of high integration, low power, low cost and good design. Mismatch in the load capacitors can lead to offset in the comparator it will consume more power [2]. The high speed comparators will lead the supply voltage becomes larger [3], [4]. Many techniques, such as supply boosting methods [6], [7], techniques employing body-driven transistors [8], [9], current-mode design [10] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. The fastest and more power efficient comparators generate more kickback noise. Minimizing kickback noise is the complex process and it will require more power [11].

In this paper, a comprehensive analysis on delay, power consumption and area of the dynamic comparator with different architecture will be presented. A new dynamic comparator is presented based on the double-tail structure which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional dynamic comparator, latch delay time is profoundly reduced. This modification also

results in considerable power savings when compared to the conventional comparators.

II. LITERATURE SURVEY

Okaniwa (2005) [12] proposed a differential comparator that can sample 40-Gb/s signals and that operates off a single 1.2-V supply was designed and fabricated in 0.11-μm standard CMOS technology. It consists of a front-end sampler, a regenerative stage, and a clocked amplifier to provide a small aperture time and a high toggle rate. The clocked amplifier employs a bandwidth modulation technique that switches the feedback gain to reduce the reset time while keeping the effective gain high. It was confirmed that the comparator receives a 40-Gb/s data stream at a toggle rate of 10 GHz with bit error rate less than 10-12 by laboratory measurements.

Goll and Zimmermann (2007) [13] presented a comparator, fabricated in a 1.5 V/0.12 mum CMOS process, was presented. The commonly separated reset and active load transistors of typical comparators are combined. In the input part two NMOS transistors are added to reduce power consumption. At a supply voltage of 0.5 V the comparator works at a maximal clock of 600 MHz and consumes 18 μW.

Nikoozadeh and Murmann (2006) [15] presented a briefly analyzes the effect of load capacitor mismatch on the offset of a regenerative latch comparator. Two analytical models are presented and compared with HSpice simulations. Results indicate that in a typical 0.18-mum CMOS latch, a capacitive imbalance of only 1fF can lead to offsets of several tens of mV.

Figueiredo and Vital (2006) [16] proposed a latched comparator is a building block of virtually all analog-to-digital converter architectures. It uses a positive feedback Mechanism to regenerate the analog input signal into a full-scale digital level. The large voltage variations in the internal nodes are coupled to the input, disturbing the input voltage-this is usually called kickback noise. This briefly reviews existing solutions to minimize the kickback noise and proposes two new ones. HSPICE simulations of comparators implemented in a 0.18-μm technology demonstrate their effectiveness.

III. PROPOSED METHODOLOGY

The schematic diagram of the proposed dynamic double tail comparator is shown in the Fig. 7.with two nMOS switches (Mn1 and Mn2) added to the switching transistors (Msw1 and Msw2) in order to reduce the static power consumption. This circuit works similar to the previous comparator structure. This circuit uses the power gating technique to reduce the static power consumption. The additional transistors switches when it has high input voltage otherwise it remains in the off state and reduces power consumption by grounding the static power consumed. In addition to reducing the stand-by power, power gating has the merit of enabling iddq testing.

A. Proposed Dynamic Comparator

Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (MC1 and MC2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner.

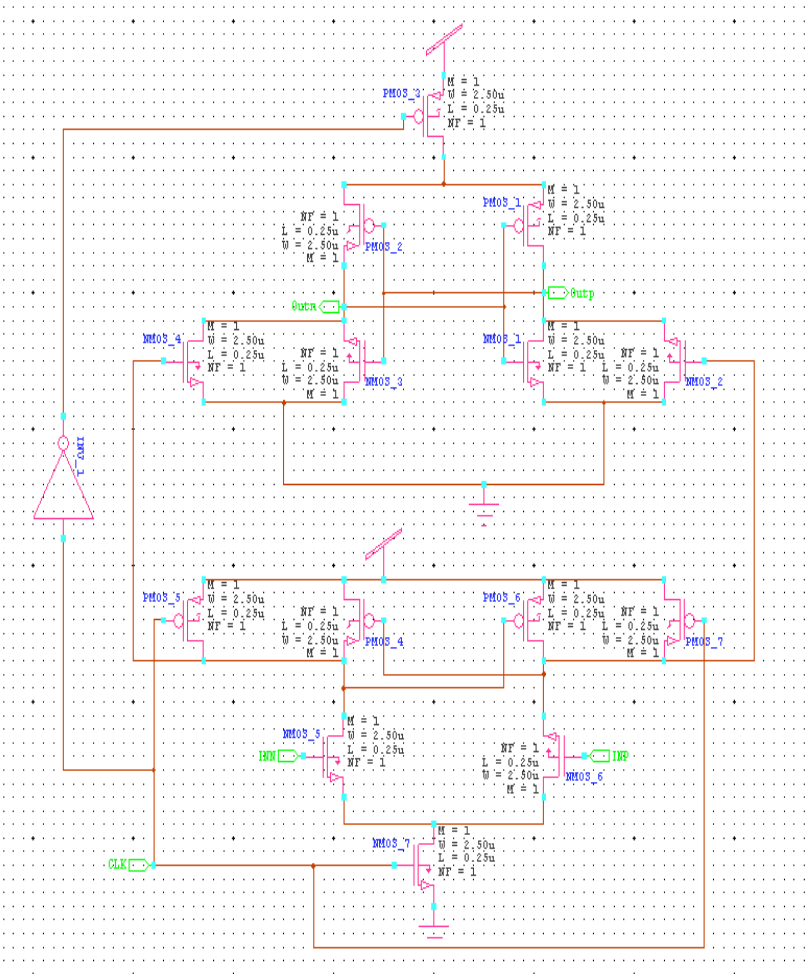

Figure 1: Proposed Dynamic Comparator

The operation of the proposed comparator is as follows.

- During reset phase (CLK =0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor MC1 and MC2 are cut off.
- Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off.
- Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD).
- Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1).
- As long as fn continues falling, the corresponding PMOS control transistor (MC1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (MC2) remains off, allowing fn to be discharged completely.
- In other words, unlike conventional double-tail dynamic comparator, in which ΔVfn/fp is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD.
- Therefore as time passes, the difference between fn and fp (ΔVfn/fp) increases in an exponential

manner, leading to the reduction of latch regeneration time.

Modified Dynamic Comparator

Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., MC1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., MC1, M1, and Mtail1), resulting in static power consumption. To overcome this issue, two NMOS switches are used below the input transistors [Msw1 and Msw2, as shown in Fig 4.2]. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. If that fp is pulling up to the VDD and fn should be discharged completely, then the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node

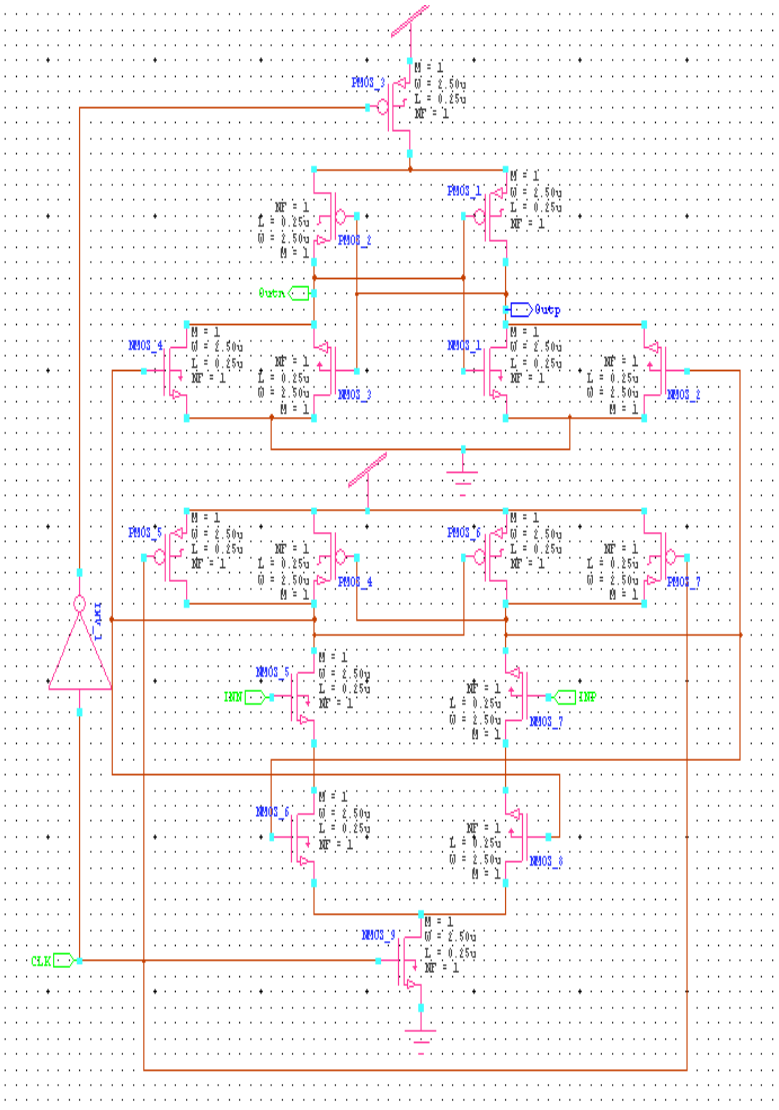

Figure 2: Modified Dynamic Comparator

In other words, the operation of the control transistors with the switches emulates the operation of the latch.

B. Delay Analysis

The analysis is similar to the conventional double-tail dynamic comparator, however, the proposed dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference (ΔV0) at the beginning of the regeneration (t = t0); and second, it enhances the effective transconductance (gmeff) of the latch. Each of these factors will be discussed in detail.

1. Effect of enhancing ΔV0: As discussed before, we define t0, as a time after which latch regeneration starts. In other words, t0 is considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the back-to-back inverters turns on, so that it will pull down one of the outputs and regeneration will commence. The latch output voltage difference at time t0, (ΔV0) has a considerable impact on the latch regeneration time, such that bigger ΔV0 results in less regeneration time. Similar to the equation derived for the ΔV0 of the double-tail structure, in this comparator we have

$$\Delta V_0 = V_{thn}\frac{\Delta Ilatch}{IB1}$$

$$\approx 2V_{thn}\frac{\Delta Ilatch}{I_{tail\,2}}$$

$$= 2V_{thn}\frac{g_m R1,2}{I_{tail\,2}}\Delta V_{f_{n/f_p}} \qquad (1)$$

In order to find ΔVfn/fp at t = t0, we shall notice that the combination of the control transistors Mc1 and Mc2) with two serial switches (Msw1, Msw2) emulates the operation of a back- to-back inverter pair; thus using small-signal model, ΔVfn/fp is calculated by

$$\Delta V_{f_{n/f_p}} = \Delta V_{f_n}(p)0\exp((A_V - 1)\mathrm{t}/\tau \qquad (2)$$

In this equation, τ /Av−1 ∼ CL,fn(p) /Gm,eff1 and ΔVfn(p)0 is the initial fn/fp node difference voltage at the time when the corresponding pMOS control transistor is started to be turned on. Hence, it can be shown that ΔVfn(p)0 is obtained from

$$\Delta V_{f_n}(p)0 = 2\left|V_{hp}\right|\frac{g_m R1,2}{I_{tail\,1}} \qquad (3)$$

Substituting (2) in (1), ΔV0 will be

$$\Delta V_0 = 2V_{thn}\frac{g_m 1,2\Delta V_{in}}{I_{tail\,2}}\Delta V_{f_{n/f_p}}$$

$$= 4\left|V_{hp}\right|\frac{g_m R1,2}{I_{tail\,2}}\frac{g_m R1,2}{I_{tail\,1}}\exp\left(\frac{g_m,eff\,1.t_0}{CL,f_n(p)}\right. \qquad (4)$$

Comparing (5) with (10), it is evident that ΔV0 has been increased remarkably (in an exponential manner) in compare with the conventional dynamic comparator.

2. Effect of Enhancing Latch Effective Transconductance: As mentioned before, in conventional double-tail comparator, both fn and fp nodes will be finally discharged completely. In our proposed comparator, however, the fact that one of the first stage output nodes (fn/fp) will charge up back to the VDD at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective Transconductance of the latch is increased. In other words, positive feedback is strengthened. Hence, tlatch will be

$$tlatch = \frac{CL_{out}}{g_m,eff + g_m R1,2}.\ln(\frac{\Delta V_{out}}{\Delta V_0}) \qquad (5)$$

Finally, by including both effects, the total delay of the proposed comparator is

$$tdelay = t_0 + tlatch$$

$$= \frac{2V_{thn}CL_{out}}{I_{tail\,2}} + \frac{CL_{out}}{g_m,eff + g_m R1,2}.\ln(\frac{VDD/2}{\Delta V_0}) \qquad (6)$$

By comparing the expressions derived for the delay of the three mentioned structures, it can be seen that the proposed comparator takes advantage of

an inner positive feedback in double-tail operation, which strengthen the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of VTh/VDD, the transconductance of the transistors decreases, thus the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator. Simulation results confirm this matter.3) Reducing the Energy Per Comparison: It is not only the delay parameter which is improved in the modified proposed comparator, but the energy per conversion is reduced as well. As discussed earlier, in conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the VDD. However, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required.

C. Design Considerations

In designing the proposed comparator, some design issues must be considered. When determining the size of tail transistors (Mtail1 and Mtail2), it is necessary to ensure that the time it takes that one of the control transistors turns on must be smaller than t0 (start of regeneration)

$$t_{on,}M_C1 < t_{0\rightarrow}\frac{|V_{thp}|.CL,f_n(p)}{ln1,2} < \frac{V_{thn}CL_{out}}{IB1} \quad (7)$$

This condition can be easily achieved by properly designing the first and second stage tail currents. Even if possible in the fabrication technology, low-threshold pMOS devices can be used as control transistors leading to faster turn on. In designing the nMOS switches, located below the input transistors, the drain-source voltage of these switches must be considered since it might limit the voltage headroom, restricting the advantage of being used in low-voltage applications. In order to diminish this effect, low-on-resistance nMOS switches are required. In other words, large transistors must be used. Since the parasitic capacitances of these switches do not affect the parasitic capacitances of the fn/fp nodes (delay bottlenecks), it is possible to optimally select the size of the nMOS switch transistors in a way that both low-voltage and low-power operations are maintained. The effect of mismatch between controlling transistors on the total input-referred offset of the comparator is another important issue. When determining the size of controlling transistors (MC1 − MC2), two important issues should be considered. First, the effect of threshold voltage mismatch and current factor mismatch of the controlling transistors on the comparator input-referred offset voltage. Second, the effect of transistor sizing on parasitic capacitances of the fn/fp nodes, i.e., CL,fn(p), and consequently the delay of the comparator. While larger transistors are required for better matching; however, the increased parasitic capacitances are delay bottlenecks. In order to study the effect of threshold and current factor mismatch of control transistors on the total input-referred offset voltage, a brief mismatch analysis is presented here.

Mismatch Analysis

In principle, the effect of threshold voltage mismatch and current factor mismatch of controlling transistors is almost negligible in most cases except for the situation where input differential voltage (ΔVin) is very small where fn and fp have approximately similar discharging rates. This is true because by the time that the controlling transistor (Mc1 or MC2) turns on, the differential input signal is already amplified to large amplitude compared to the mismatches. In other words, offset due to the controlling transistor mismatches is divided by the gain from the input to the output. However, in case of small ΔVin, when fn and fp follow each other tightly, the mismatch of the controlling transistors might influence

the result of the comparison. Hence, the following brief analyzes the effect of threshold and current factor mismatches of controlling transistors on the total input-referred offset voltage.

Effect of Threshold Voltage Mismatch of MC1, MC2, i.e., ΔVThC1,2: The differential current due to the threshold voltage mis- match can be obtained from

$$Idiff = g_{mc}\,1{,}2\Delta VThc1{,}2 \qquad (8)$$

where gmc1,2 is the transconductance of the controlling transistors. So, the input referred offset voltage due to the Mc1,2 threshold voltage mismatch is obtained as follows:

$$\Delta V_{eq}, due_{\Delta Thc1,2} = \frac{g_{mc}\,1{,}2\Delta VThc1{,}2}{g_m\,1{,}2} \qquad (9)$$

where VOD refers to the overdrive voltage of the transistors.

Effect of Current-Factor Mismatch MC1, MC2, i.e., ΔβC1,2: In order to calculate the input-referred offset due to the current factor mismatch of MC1,2, ΔβC1,2 is modelled as a channel width mismatch ΔW, i.e., Δβ/β = ΔW/W. The differential current that ΔW generates can be obtained as expressed in (10).

$$Idiff = \frac{1}{2}\mu C_{ox}\,\frac{\Delta W}{L}\,(V_{gsc}\,1{,}2 - V_{thcc}\,1{,}2) \qquad (10)$$

The controlling transistors are in saturation since |VGDc1,2|=| Vfn −Vfp| < |Vthp|. So the input-referred offset voltage due to the current factor mismatch is calculated from

$$\Delta V_{eq,} due_{\Delta Bc1,2} = \frac{Idiff}{g_m\,1{,}2} \qquad (11)$$

where Vcm is the input common mode voltage and Rclk is the equivalent on resistance of the tail transistor. Assuming both mismatch factors, the total input-referred offset due to the mismatch of the controlling transistors can be found from

$$\sigma total = \sqrt{(\sigma^2{}_{\Delta Vthc1,2} + \sigma^2{}_{\Delta Vthc1,2}} \qquad (12)$$

From (9) and (10), it can be concluded that the ratio of the controlling transistor sizes to the input transistor size, i.e., (WC1,2/W1,2), is effective in reducing the offset. Due to the fact that the transconductance of the input transistors (gm1,2) is important in amplifying the input differential voltage and due to the dominant role of the size of these transistors on total input-referred offset, usually large input transistors are designed, which results in diminishing the effect of controlling transistors mismatch.

Kickback Noise

Principally in latched comparators, the large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called "kickback noise." Fastest and most power efficient comparators generate more kickback noise. This is true about our proposed dynamic comparator. Although it improves the double-tail topology in terms of operation speed and thus energy per comparison, the kickback noise is increased in comparison to conventional double-tail structure. Fig. 4.5 presents the peak disturbance as a function of differential input voltage of the comparator in three studied architectures. While double-tail structure takes advantage of input-output isolation and thus the minimum 20 kickback noise, the conventional dynamic comparator and our proposed structure has nearly similar kickback noise. However, in our proposed comparator since control transistors are not supposed to be as strong as the latch transistors in conventional dynamic comparator, it is possible to determine the size of those transistors in a way that keeps the advantages of the speed enhancement and power reduction, while reducing kickback noise. Besides, for some applications where kickback becomes important, it is possible to apply simple kickback reduction techniques, such as neutralization to remarkably reduce the

kickback noise (proposed dynamic comparator with neutralization).

IV. EXPERIMENTAL RESULTS

This section deals with simulation results and discussions of the Dynamic Comparators. The software tool used is TANNER. The simulation and power analysis is obtained with the help of TANNER tool, using 130nm technology.

Comparator Analysis

Conventional Dynamic Comparator

The simulation result of the Conventional Dynamic Comparator is shown in Fig. 3 and Fig 4 has the inputs INN and INP which is applied to the transistors M1 and M2 and the clock signals given to the transistors M7, M8 and Mtail. Comparator compares two input signals and gives output which indicates the high or low input value. The output signals obtained by the comparison of two inputs are also shown. The functional verification is done by using TANNER tool.

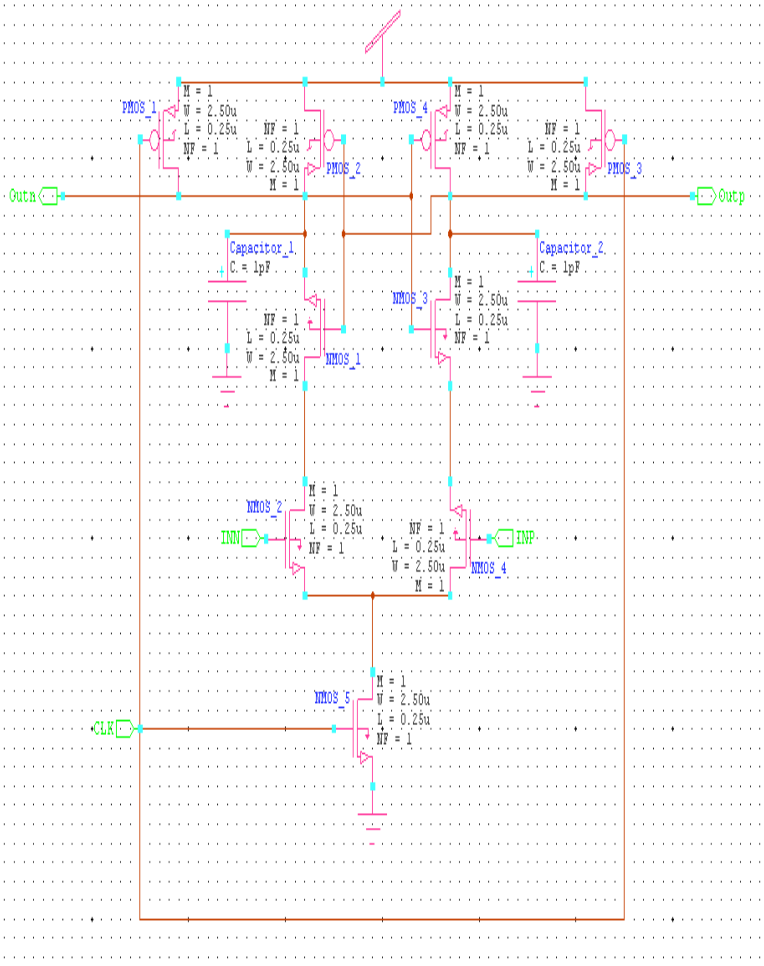

Figure 3: Conventional Dynamic Comparator

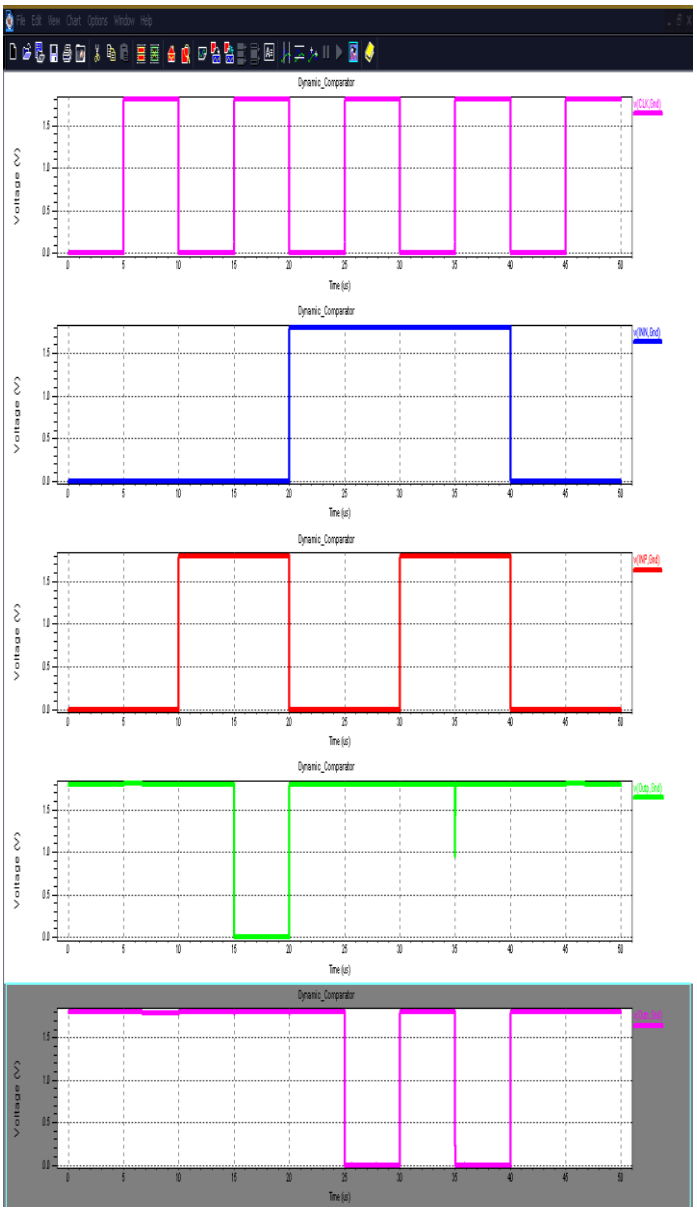

Figure 4: Simulation for Conventional Dynamic Comparator

When VINP is greater than VINN, Outn is pulled to VDD and Outp discharges to ground. When VINN is greater than VINP, Outp is pulled to VDD and Outp discharges to ground.

Conventional Double Tail Dynamic Comparator

The simulation result of the Conventional Dynamic Comparator is shown in Fig. 5 and Fig. 6 has the inputs INN and INP which is applied to the transistors M1 and M2, the clock signals given to the transistors M3, M4 and Mtail1 and clock bar signal given to Mtail2. Comparator compares two input signals and gives output which indicates the high or low input value. The output signals obtained by the comparison of two inputs are also shown. The functional verification is done by using TANNER tool.

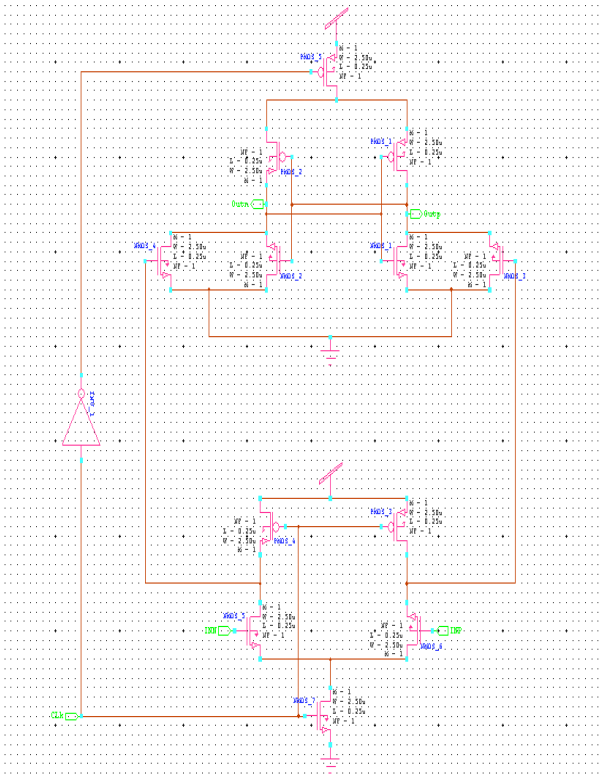

Figure 5: Conventional double-tail Dynamic Comparator

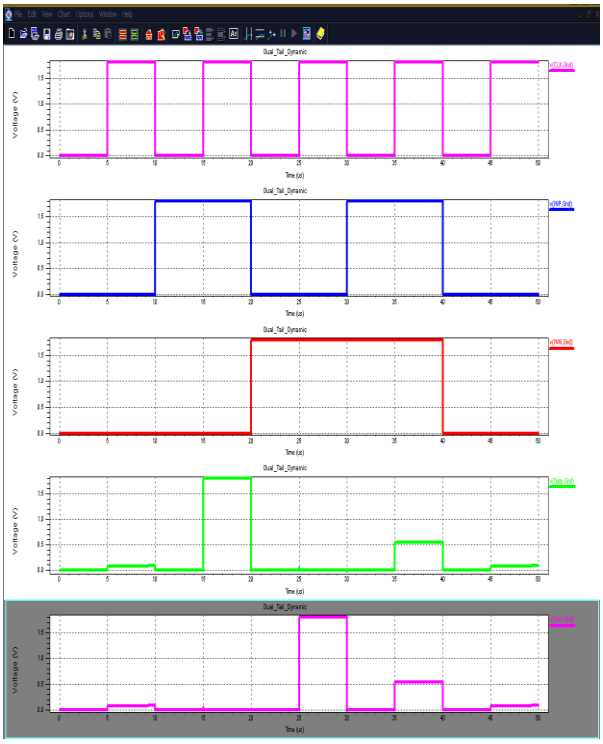

Figure 6: Simulation for Conventional Double Tail Dynamic Comparator

When VINP is greater than VINN, Outn is pulled to ground and Outp discharges to VDD. When VINN is greater than VINP, Outp is pulled to ground and Outp discharges to VDD.

Proposed Dynamic Comparator

The simulation result of the Conventional Dynamic Comparator is shown in Fig. 7 and Fig. 8 has the inputs INN and INP which is applied to the transistors M1 and M2, the clock signals given to the transistors M3, M4 and Mtail1 and clock bar signal given to Mtail2. Comparator compares two input signals and gives output which indicates the high or low input value. The output signals fp, fn, Outp and Outn obtained by the comparison of two inputs are also shown. The functional verification is done by using TANNER tool. When VINP is greater than VINN, Outn is pulled to ground and Outp discharges to VDD. When VINN is greater than VINP, Outp is pulled to ground and Outp discharges to VDD.

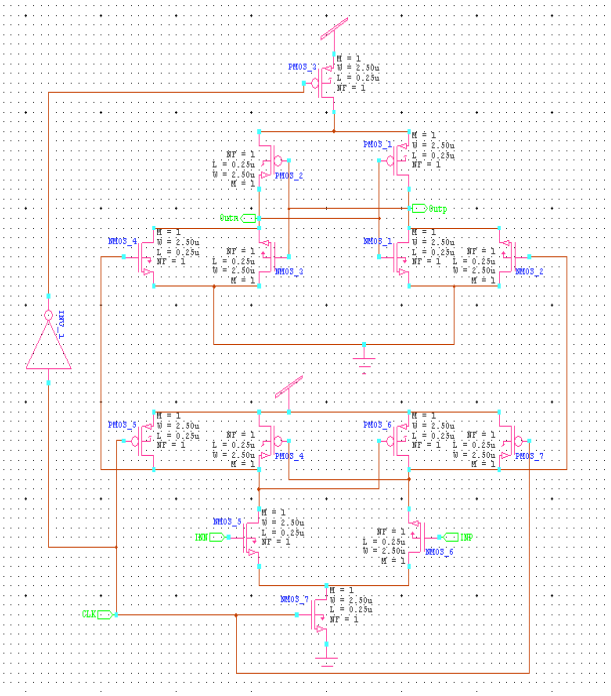

Figure 7: Proposed Dynamic Comparator

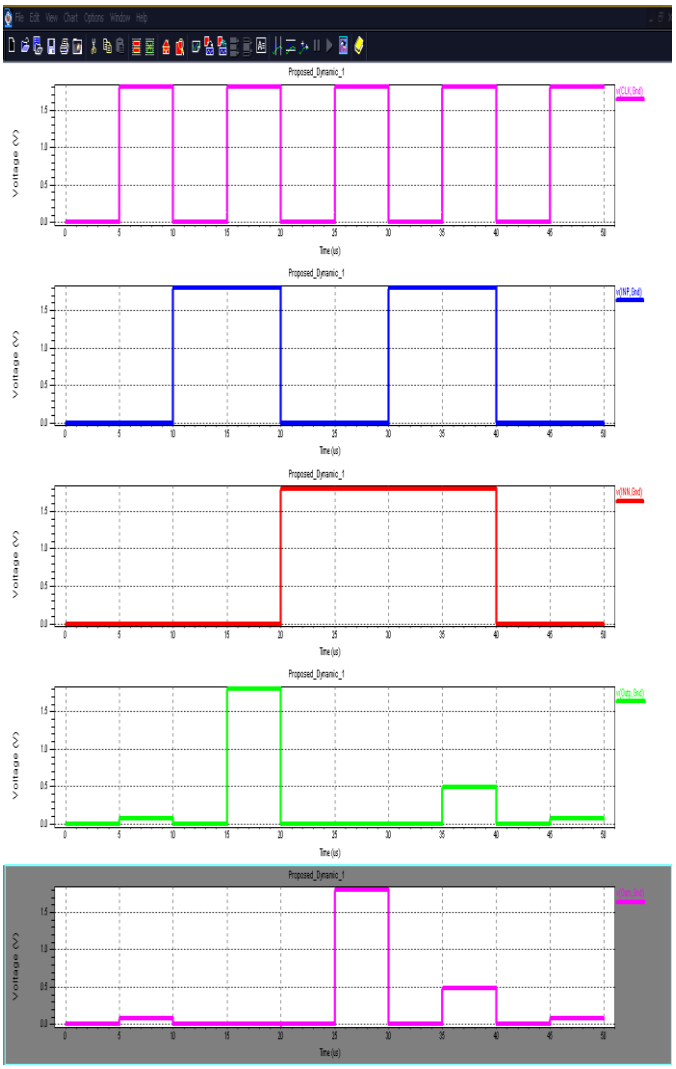

Figure 8: Simulation for Proposed Dynamic Comparator

Modified Dynamic Comparator

The simulation result of the Conventional Dynamic Comparator is shown in Fig. 9 and 10 has the inputs INN and INP which is applied to the transistors M1 and M2, the clock signals given to the transistors M3, M4 and Mtail1 and clock bar signal given to Mtail2. Comparator compares two input signals and gives output which indicates the high or low input value. The output signals fp, fn, Outp and Outn obtained by the comparison of two inputs are also shown. The functional verification is done by using TANNER tool. When VINP is greater than VINN, Outn is pulled to ground and Outp discharges to VDD. When VINN is greater than VINP, Outp is pulled to ground and Outp discharges to VDD.

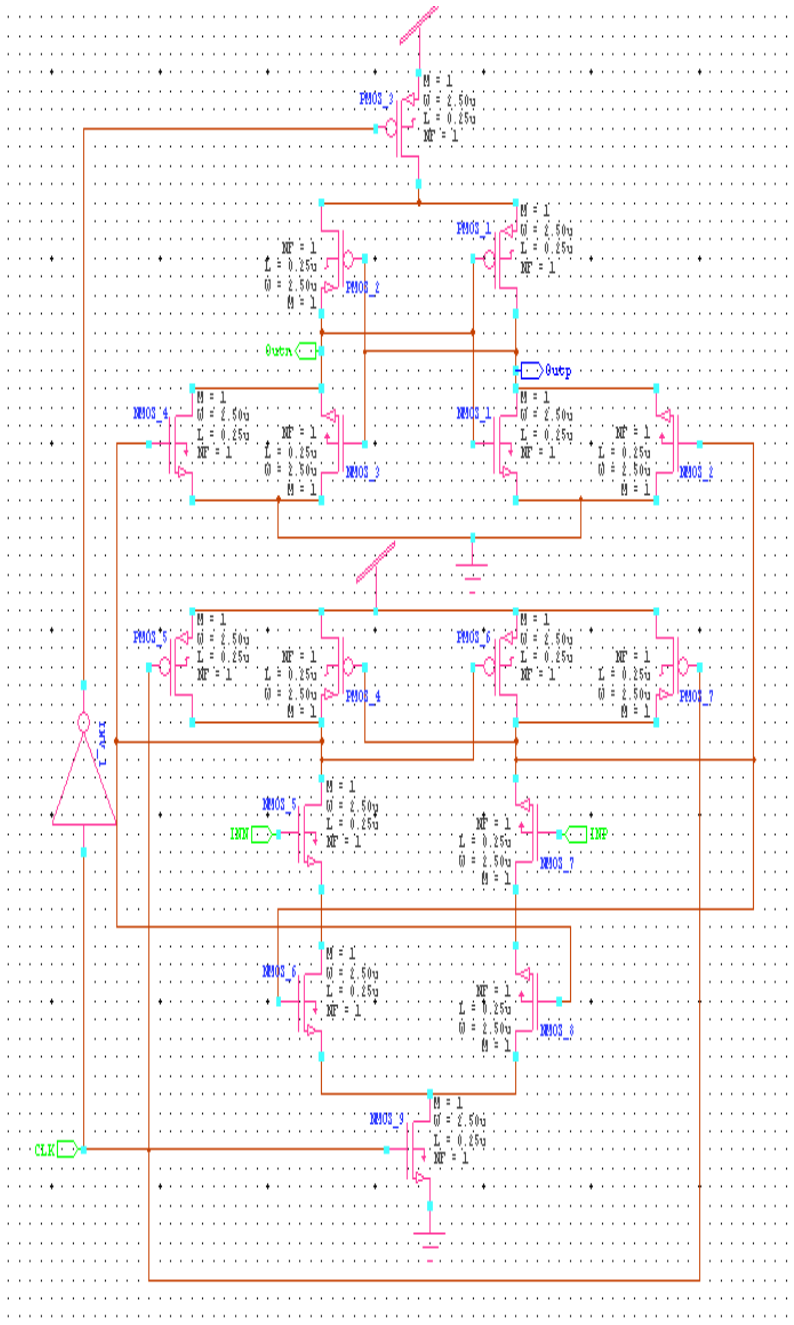

Figure 9: Modified Double-tail Comparator

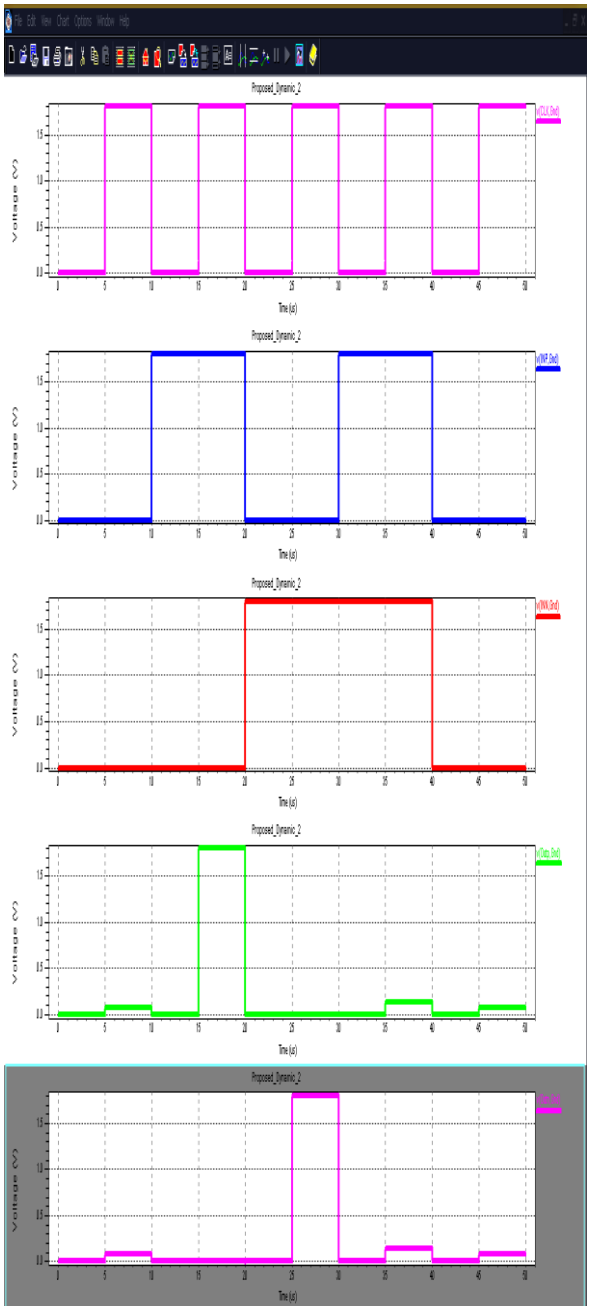

Figure 10: Simulation for Modified Dynamic Comparator

Power Analysis

Conventional Dynamic Comparator

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 4.243843e-005  1.7993e+000  1.8000e+000  0.0000e+000  0.0000e+000  0.0000e+000
 4.500000e-005  1.8007e+000  1.8000e+000  0.0000e+000  0.0000e+000  0.0000e+000
 4.5001000e-005  1.8066e+000  1.8058e+000  0.0000e+000  0.0000e+000  1.8000e+000
 4.5001315Oe-005  1.8066e+000  1.8058e+000  0.0000e+000  0.0000e+000  1.8000e+000
 4.5004465e-005  1.8066e+000  1.8058e+000  0.0000e+000  0.0000e+000  1.8000e+000
 4.503596e-005  1.8066e+000  1.8058e+000  0.0000e+000  0.0000e+000  1.8000e+000
 4.528884e-005  1.8063e+000  1.8055e+000  0.0000e+000  0.0000e+000  1.8000e+000
 4.623839e-005  1.8045e+000  1.8038e+000  0.0000e+000  0.0000e+000  1.8000e+000
 4.671316e-005  1.8037e+000  1.8029e+000  0.0000e+000  0.0000e+000  1.8000e+000
 5.000000e-005  1.7977e+000  1.7970e+000  0.0000e+000  0.0000e+000  1.8000e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
V1 from time 0 to 5e-005
Average power consumed -> 2.380021e-007 watts
Max power 1.086175e-003 at time 4.0001e-005
Min power 1.423380e-011 at time 4.62384e-005


* END NON-GRAPHICAL DATA
*

* Parsing                  0.01 seconds
* Setup                    0.02 seconds
* DC operating point       0.00 seconds
* Transient Analysis       0.03 seconds
* Overhead                 1.50 seconds
* ------------------------------------
* Total                    1.56 seconds

* Simulation completed  with  7 Warnings

* End of T-Spice output file
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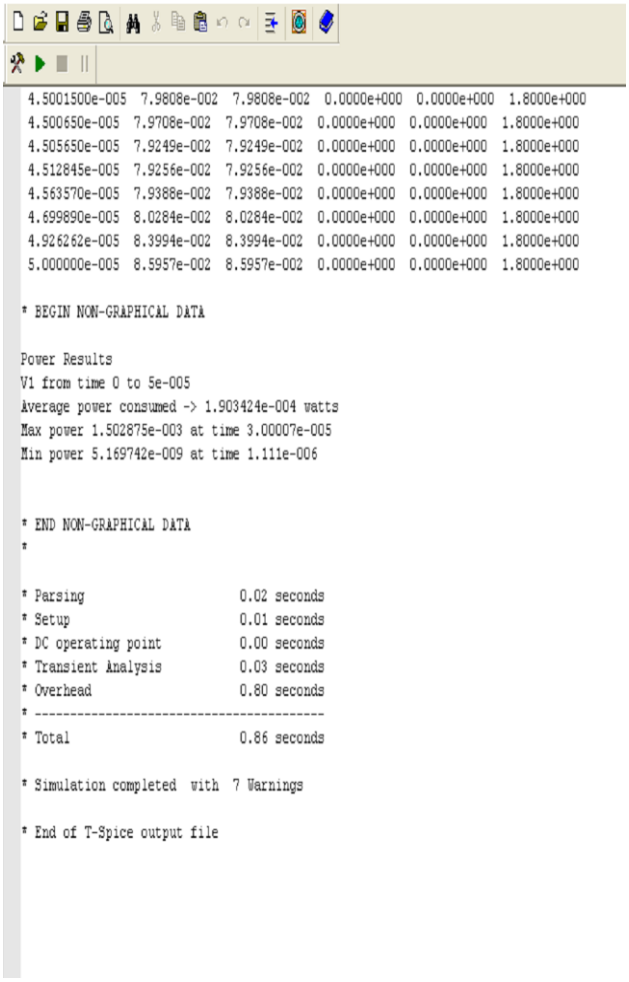
Figure 11: Power Results for Conventional Dynamic Comparator

The power result of the Conventional Dynamic Comparator is been analyzed using TANNER Tool and shown in Fig. 11. The average power consumption is 2.3800µW. The maximum and minimum powers consumed are 1.0861mW and 1.4233pW with respect to switching activities of transistors in M3and M4**.**

Conventional Double Tail Dynamic Comparator



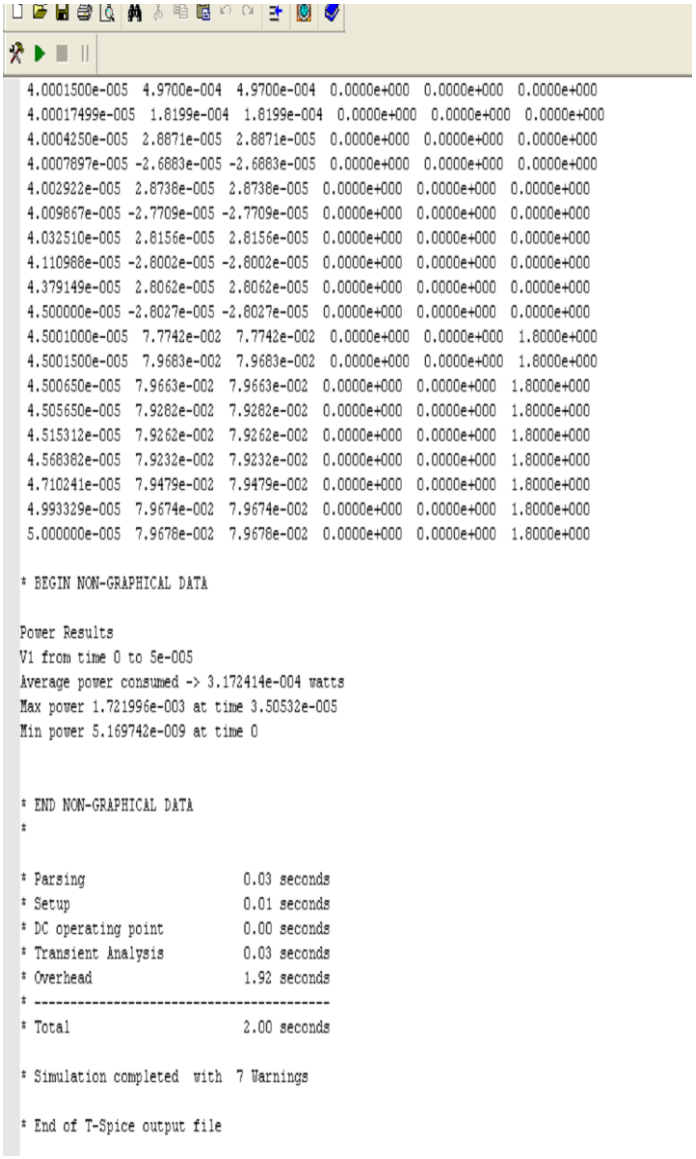
```
4.5001500e-005  7.9808e-002  7.9808e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.500650e-005  7.9708e-002  7.9708e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.505650e-005  7.9249e-002  7.9249e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.512845e-005  7.9256e-002  7.9256e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.563570e-005  7.9388e-002  7.9388e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.699890e-005  8.0284e-002  8.0284e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.926262e-005  8.3994e-002  8.3994e-002  0.0000e+000  0.0000e+000  1.8000e+000
5.000000e-005  8.5957e-002  8.5957e-002  0.0000e+000  0.0000e+000  1.8000e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
V1 from time 0 to 5e-005
Average power consumed -> 1.903424e-004 watts
Max power 1.502875e-003 at time 3.00007e-005
Min power 5.169742e-009 at time 1.111e-006


* END NON-GRAPHICAL DATA
*

* Parsing                    0.02 seconds
* Setup                      0.01 seconds
* DC operating point         0.00 seconds
* Transient Analysis         0.03 seconds
* Overhead                   0.80 seconds
* ----------------------------------------
* Total                      0.86 seconds

* Simulation completed  with  7 Warnings

* End of T-Spice output file
```

Figure 12: Power Results for Conventional Double Tail Dynamic Comparator

The power result of the Conventional Double Tail Dynamic Comparator is been analyzed using TANNER Tool and shown in Fig. 12. The average power consumption is 1.9034µW. The maximum and minimum powers consumed are 1.5028mW and 5.1697pW respect to switching activities of clocked transistors in Mtail1and Mtail2 reduced the power dissipation at MR1 and MR2.

Proposed Dynamic Comparator

The power result of the Conventional Double Tail Dynamic Comparator is been analyzed using TANNER Tool and shown in Fig. 13. The average power consumption is 3.1724µW. The maximum and minimum powers consumed are 1.7219mW and 5.1697pW switching activities of clocked transistors in Mtail1and Mtail2 are controlled MC1and MC2 through fp, fn due to that reduce the power dissipation.

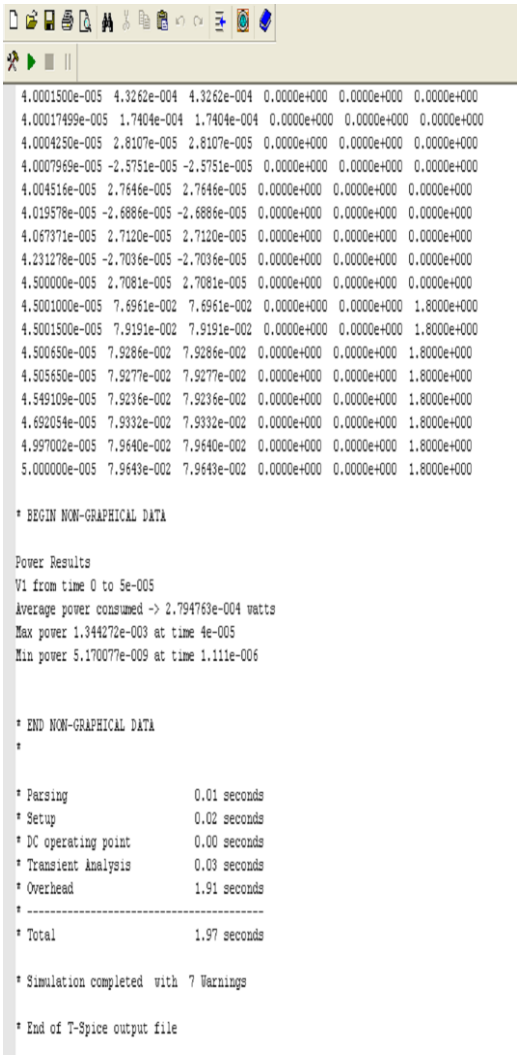


```
4.0001500e-005  4.9700e-004  4.9700e-004  0.0000e+000  0.0000e+000  0.0000e+000
4.00017499e-005  1.8199e-004  1.8199e-004  0.0000e+000  0.0000e+000  0.0000e+000
4.0004250e-005  2.8871e-005  2.8871e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.0007897e-005 -2.6883e-005 -2.6883e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.002922e-005  2.8738e-005  2.8738e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.009867e-005 -2.7709e-005 -2.7709e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.032510e-005  2.8156e-005  2.8156e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.110988e-005 -2.8002e-005 -2.8002e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.379149e-005  2.8062e-005  2.8062e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.500000e-005 -2.8027e-005 -2.8027e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.5001000e-005  7.7742e-002  7.7742e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.5001500e-005  7.9683e-002  7.9683e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.500650e-005  7.9663e-002  7.9663e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.505650e-005  7.9282e-002  7.9282e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.515312e-005  7.9262e-002  7.9262e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.568382e-005  7.9232e-002  7.9232e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.710241e-005  7.9479e-002  7.9479e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.993329e-005  7.9674e-002  7.9674e-002  0.0000e+000  0.0000e+000  1.8000e+000
5.000000e-005  7.9678e-002  7.9678e-002  0.0000e+000  0.0000e+000  1.8000e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
V1 from time 0 to 5e-005
Average power consumed -> 3.172414e-004 watts
Max power 1.721996e-003 at time 3.50532e-005
Min power 5.169742e-009 at time 0


* END NON-GRAPHICAL DATA
*

* Parsing                    0.03 seconds
* Setup                      0.01 seconds
* DC operating point         0.00 seconds
* Transient Analysis         0.03 seconds
* Overhead                   1.92 seconds
* ----------------------------------------
* Total                      2.00 seconds

* Simulation completed  with  7 Warnings

* End of T-Spice output file
```

Figure 13: Power Results for Proposed Dynamic Comparator

Modified Dynamic Comparator

The power result of the Double Tail Dynamic Comparator is been analyzed using TANNER Tool and shown in Fig 14. The average power consumption is 2.7947µW.The maximum and minimum Powers consumed are 1.3442mW and 5.1700pW switching activities of clocked transistors in Mtail1 and Mtail2 transistor are reduced the power consumption.



```
4.0001500e-005  4.3262e-004  4.3262e-004  0.0000e+000  0.0000e+000  0.0000e+000
4.0001749e-005  1.7404e-004  1.7404e-004  0.0000e+000  0.0000e+000  0.0000e+000
4.0004250e-005  2.8107e-005  2.8107e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.0007969e-005 -2.5751e-005 -2.5751e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.0045160e-005  2.7646e-005  2.7646e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.0195780e-005 -2.6886e-005 -2.6886e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.0673710e-005  2.7120e-005  2.7120e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.2312780e-005 -2.7036e-005 -2.7036e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.5000000e-005  2.7081e-005  2.7081e-005  0.0000e+000  0.0000e+000  0.0000e+000
4.5001000e-005  7.6961e-002  7.6961e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.5001500e-005  7.9191e-002  7.9191e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.5006500e-005  7.9286e-002  7.9286e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.5056500e-005  7.9277e-002  7.9277e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.5491090e-005  7.9236e-002  7.9236e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.6920540e-005  7.9332e-002  7.9332e-002  0.0000e+000  0.0000e+000  1.8000e+000
4.9970020e-005  7.9640e-002  7.9640e-002  0.0000e+000  0.0000e+000  1.8000e+000
5.0000000e-005  7.9643e-002  7.9643e-002  0.0000e+000  0.0000e+000  1.8000e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
V1 from time 0 to 5e-005
Average power consumed -> 2.794763e-004 watts
Max power 1.344272e-003 at time 4e-005
Min power 5.170077e-009 at time 1.111e-006


* END NON-GRAPHICAL DATA
*

* Parsing                  0.01 seconds
* Setup                    0.02 seconds
* DC operating point       0.00 seconds
* Transient Analysis       0.03 seconds
* Overhead                 1.91 seconds
* ----------------------------------------
* Total                    1.97 seconds

* Simulation completed  with  7 Warnings

* End of T-Spice output file
```

Figure 14 Power Results for Modified Dynamic Comparator

Table 1: Parameter Analysis

Parameter	Single tail Conventional	Dual tail Conventional	Proposed Dual tail	Modified dual tail
Average Power consumption (uw)	2.3800	1.9034	3.1724	2.7947
Static power (mw)	1.0861	1.5028	1.7219	1.3442
No. Of clocked transistor	3	4	4	4
PDP (nws)	5.4305	7.514	8.6095	6.721
EDP (pws)	2.715	3.757	4.3070	3.3605
Frequency (hz)	0.02	0.02	0.02	0.02
No of transistor	9	12	14	16

The simulations and the power analysis of the comparators are done using TANNER which portrays the objective efficiently with 130nm technology scaling. The Double Tail Dynamic Comparator consumed low power when compared to conventional Dynamic Comparator. It is found that the Modified double-tail comparator consumed 0.377 mW less than the Double Tail Dynamic comparator.

V. CONCLUSION

A comprehensive delay analysis for clocked dynamic comparators is presented. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analysed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low power capability is proposed in order to improve the performance of the comparator. Simulation results in 0.13-μm CMOS technology confirmed that the delay and power consumption of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). The need for ultra low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. So in ultra low-power, area efficient and high speed analog-to-digital converters can use the proposed comparators. Many high- speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. In future the proposed comparator can apply in high-speed ADCs, such as flash ADCs to improve the performance.

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