A Transformerless Single-Stage Single Switch AC/DC Converter with High Power Factor, Regulated Bus and Output Voltages

Preethy G Nair and K.V. Loveleen

Abstract--- This paper presents a transformerless single-stage single switch AC/DC converter with direct power transfer and high power factor suitable for universal line applications (90-270Vrms).Unlike existing single-stage ac/dc converters with uncontrolled intermediate bus voltage, a new high step-down transformerless single-stage single switch ac/dc converter achieving intermediate bus voltage regulation and output voltage regulation is proposed. With the direct power transfer feature, the converter is able to achieve efficient power conversion, high power factor correction, low voltage stress on intermediate bus (less than 120V) and low output voltage. The topology integrates a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. A detailed analysis of the proposed converter for regulated intermediate bus voltage and output voltage with simulation results are presented. From experimental set up we obtain 12V output by giving 230V as input.

Keywords--- Integrated Buck-Buck-Boost Converter (IBuBuBo), Direct Power Transfer(DPT), Power-factor Correction (PFC), Single-stage (SS), Transformerless

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I. INTRODUCTION

Due to the stringent current-harmonic regulations, which are imposed on single phase ac/dc power supplies, inclusion of a power-factor-correction (PFC) circuit in the power-supply design becomes mandatory. The research on single stage PFC ac/dc converters can be carried out by early 1990s. Single-Stage power-factor-corrected ac/dc converters, which combine a power factor correction (PFC) circuit and a dc/dc regulator circuit and share a common set of active power switches. The aims are to reduce the converter size, control circuitry, and, thus, cost. The SS ac/dc converter reduces cost, size, and complexity in the control loop by combining a PFC cell with a post-dc/dc cell and using one common set of switching-control signal. It is a very attractive solution in low power application where the manufacturing cost and size of converter are the major issues. The underlying principle for the SS ac/dc conversion is to force the PFC cell inductor operating in discontinuous conduction mode (DCM) to achieve high power factor automatically without any control loop, whereas the well and tight output regulation is done by post-dc/dc cell working in DCM or continuous conduction mode (CCM).Therefore, only one control loop is needed for the whole circuit.

Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation [1]. Their intermediate bus voltage is usually greater than the line input voltage and easily goes beyond 450 V at high-line application [2]. Also there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line

voltage due to the nature of boost-type PFC cell. In addition, the other drawbacks of the boost-type PFC cell is that it cannot limit the input inrush current and provide output short circuit protection.

Several methods were introduced to reduce the bus voltage much below the line input voltage. Several topologies have been reported [3]. Although the recently reported IBoBuBo converter [4] is able to limit the bus voltage under 400 V, it cannot be applied to the low-voltage application directly due to the boost PFC cell. On the other hand, the converters [3] employ different PFC cells to reduce the intermediate bus voltage. Among those converters, [5] use a transformer to achieve low output voltage either in PFC cell or dc/dc cell. Therefore, the leakage inductance is unavoidable. In [4], [6], the converters employ a buck–boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in [4] process power at least twice resulting in low power efficiency. Moreover, the reported converters, consist of two active switches leading to more complicated gate control. Apart from reducing the intermediate bus voltage, the converter in employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow, i.e., < 10%. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET.

To tackle the aforementioned problems, an intergrated buck–buck–boost (IBuBuBo)[7] converter with low output voltage is proposed. The topology integrates a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus (less than 130 V) and low output voltage without a high step-down transformer. The absence of transformer reduces the component counts and cost of the converter.

To sum up, the converter is able to achieve:

1. Low voltage stress on intermediate bus
2. High power factor, compact size, less cost
3. Low intermediate bus and output voltages in the absence of transformer;
4. Simple control structure with a single-switch;
5. Positive output voltage;
6. High conversion efficiency due to part of input power is processed once and
7. Input surge current protection because of series connection of input source and switch.

II. SINGLE-STAGE PFC CONVERTER

Power factor correction (PFC) techniques have become increasingly important since several regulations that are used to limit harmonic injection to the power utilities have been enacted recently. There are two basic PFC approaches, namely, active PFC and passive PFC. Active PFC, classified by the system configurations, can be categorized into two-stage and single-stage SS schemes. A two-stage scheme results in high power factor and fast response output voltage regulation by using two independent controllers and optimized power stages, as shown in Fig. 2.1(a). The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications.

An SS scheme combines the PFC cell and dc/dc power conversion cell into one stage, and typically uses only one controller and shares power switches, as shown in Fig. 2.1(b). It should be pointed out that from the viewpoint of functionality, in order to get high power factor and regulated output, an SS converter actually still needs to

complete PFC and dc/dc regulating tasks as a two-stage converter. Usually, the high power factor of an SS PFC converter is guaranteed by operating the PFC cell in discontinuous current mode (DCM), while the fast response output regulation is achieved by the dc/dc cell. Although the single-stage scheme is attractive in low cost and low power applications due to its simplified power stage and control circuit, major issues still exist, such as low efficiency and difficulty being moved to higher power level, and high as well as wide-range intermediate dc bus voltage stress.

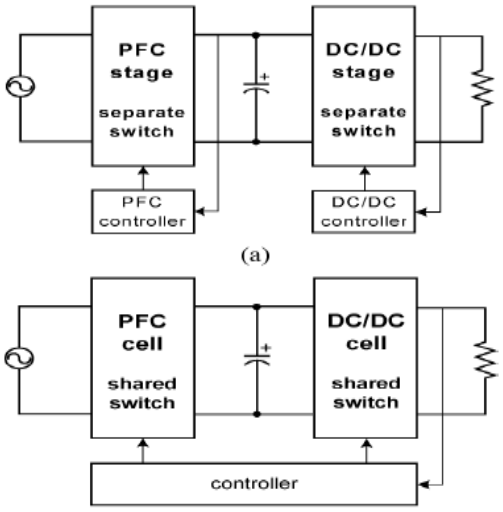


Fig. 2.1: Functional Block Diagram of PFC Converters: (a) two-stage PFC Converter (b) single-stage PFC Converter

III. PROPOSED CIRCUIT DIAGRAM AND TIS OPERATING PRINCIPLE

The topology integrates a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus (less than 130 V) and low output voltage without a high step-down transformer. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. Therefore, a transformer is not needed to obtain the low output voltage. The absence of transformer reduces the component counts and cost of the converter.

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (L_1 , S_1 , D_1 , C_o , and C_B) and a buck–boost dc/dc cell (L_2 , S_1 , D_2 , D_3 , C_o , and C_B) is illustrated in Fig. 3.1(a). Although L_2 is on the return path of the buck PFC cell, that it does not contribute to the cell electrically. Thus, L_2 is not considered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0. Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

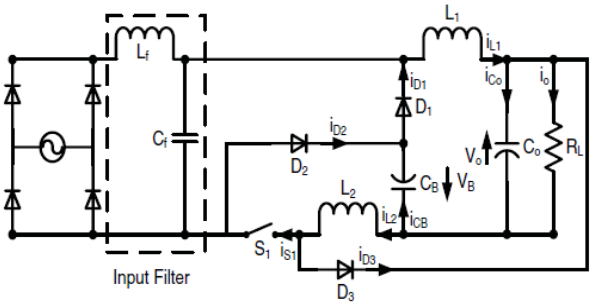


Fig. 3.1: Proposed IBuBuBo SS ac/dc Converter

3.1. Operating Principle

Mode A (v_{in} (θ)≤V_B + Vo): When the input voltage v_{in} (θ) is smaller than the sum of intermediate bus voltage V_B , and output voltage *Vo* , the buck PFC cell becomes inactive and does not shape the line current around zero crossing line voltage [20], owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 3.2

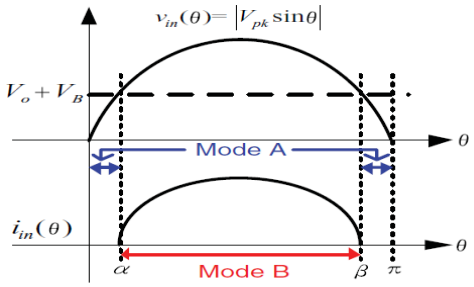


Fig. 3.2: Input Voltage and Current Waveforms

The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 3.3 (a),(b), and (f). Fig. 3.4 shows its key current waveforms.

1) Stage 1 (period d_1Ts in Fig. 3.4) [see Fig. 3.3(a)]: When switch S_1 is turned ON, inductor L_2 is charged linearly by the bus voltage V_B while diode D_2 is conducting. Output capacitor C_o delivers power to the load.
2) Stage 2 (period d_2Ts in Fig. 3.4) [see Fig. 3.3(b)]:When switch S_1 is switched OFF, diode D_3 becomes forward biased and energy stored in L_2 is released to C_o and the load.
3) Stage 3 (period d_3Ts - d_4Ts in Fig. 3.4) [see Fig. 3.3(f)]: The inductor current i_{L2} is totally discharged and only *Co* sustains the load current.

Mode B ($v_{in}(\theta) > V_B + V_o$): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 3.3 (c), (d), (e), and (f). The key waveforms are shown in Fig. 3.4.

1) Stage 1 (period d_1Ts in Fig. 3.4) [see Fig. 3.3(c)]: When switch S_1 is turned ON, both inductors L_1 and L_2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage ($v_{in}(\theta) - V_B - Vo$), while diode D_2 is conducting.
2) Stage 2 (period d_2Ts in Fig. 3.4) [see Fig. 3.3(d)]: When switch S_1 is switched OFF, inductor current i_{L1} decreases linearly to charge C_B and C_o through diode D_1 as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in L_2 is released to *Co* and the current is supplied to the load through diode D_3. This stage ends once inductor L_2 is fully discharged.
3) Stage 3 (period d_3Ts in Fig. 3.4) [see Fig. 3.3(e)]: Inductor L_1 continues to deliver current to *Co* and the load until its current reaches zero.
4) Stage 4 (period d_4Ts in Fig. 3.4) [see Fig. 3.3(f)]: Only *Co* delivers all the output power.

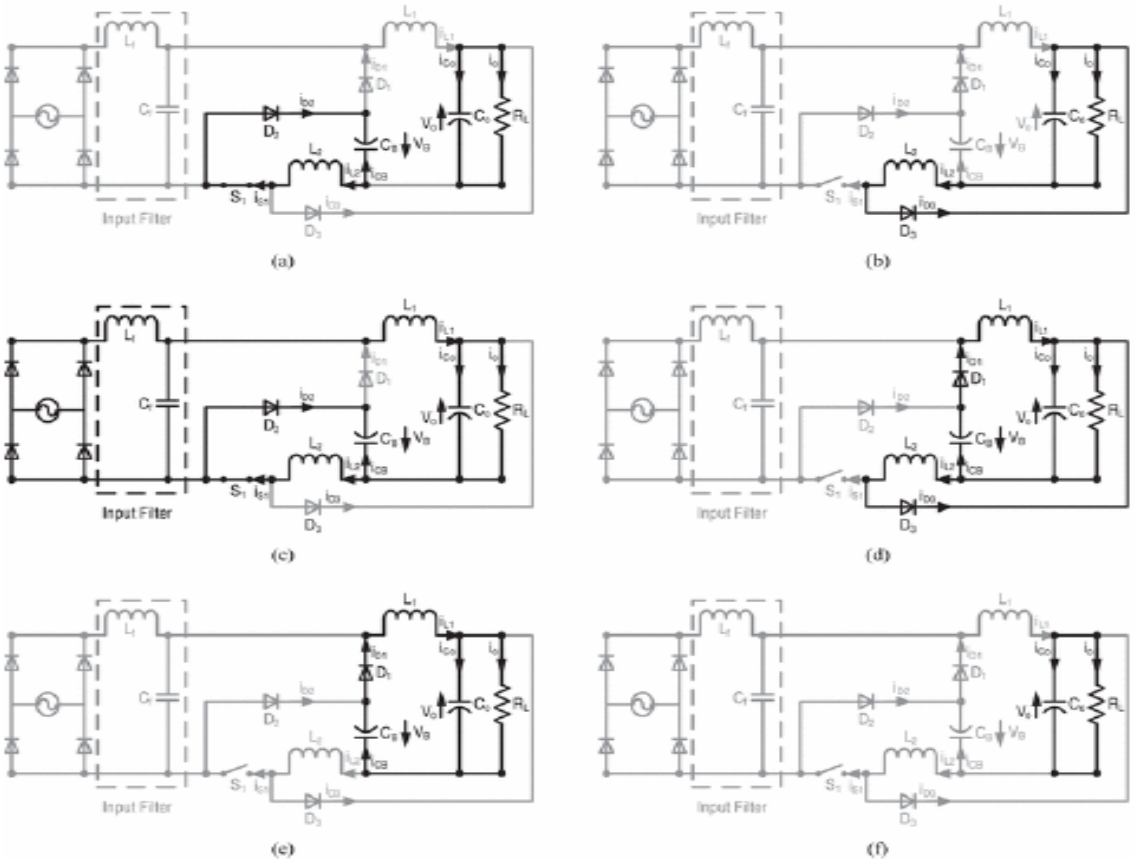


Fig. 3.3: Circuit Operation Stages of the Proposed ac/dc Converter

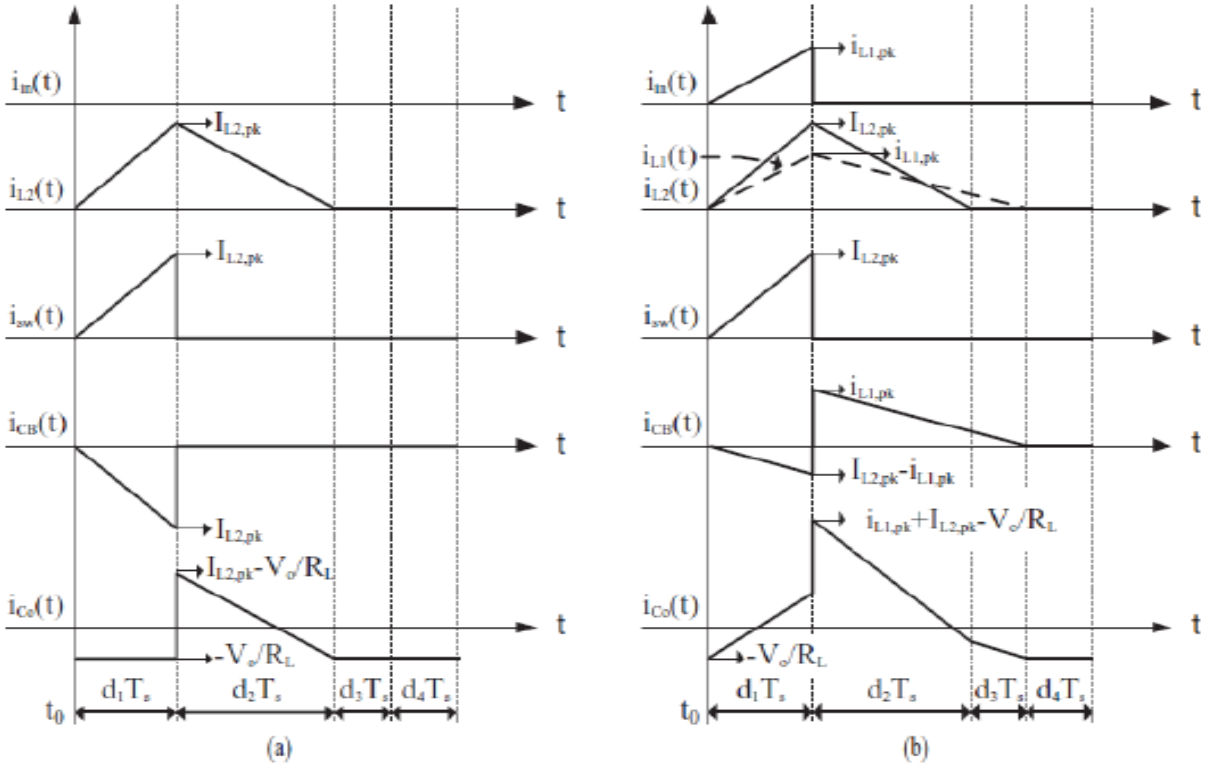


Fig. 3.4: Key Waveforms of the Proposed Circuit

IV. DESIGN CONSIDERATION

To simplify the circuit analysis, some assumptions are made as follows:

1. All components are ideal;
2. Line input source is pure sinusoidal, i.e. *v*in (θ) = *V*pk*sin*(θ) where *V*pk and θ are denoted as its peak voltage and phase angle, respectively;
3. Both capacitors C_B and *Co* are sufficiently large such that they can be treated as constant DC voltage sources without any ripples;
4. The switching frequency *fs* is much higher than the line frequency such that the rectified line input voltage |*v*in (θ)| is constant within a switching period.

4.1. Circuit Characteristics

According to Fig. 2.2, there is no input current drawn from the source in Mode A, and the phase angles of the dead-time α and β can be expressed as

$$\alpha = \arcsin(V_T \div V_{pk})$$

$$\beta = \pi - \alpha = \pi - \arcsin(V_T \div V_{pk}) \qquad (1)$$

Where V_T is the sum of V_B and *Vo* . Thus, the conduction angle of the converter is

$$\gamma = \beta - \alpha = \pi - 2\arcsin(V_T \div V_{pk}) \qquad (2)$$

From the key waveforms (see Fig. 3.4), the peak currents of the two inductors are

$$i_{L1\_pk} = \begin{cases} \frac{vin(\theta)-VT}{L1} d1Ts, & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \qquad (3)$$

And

$$I_{L2\_pk} = \frac{V_B}{L2} d_1 Ts \qquad (4)$$

where *Ts* (1/*fs*) is a switching period of the converter. In (3) and (4), the dependency of i_{L1_pk} on θ has been omitted for clarity. It is noted that L_2 does not contribute in (3) even though it is on the current return path of the PFC cell.

In addition, by considering volt–second balance of the L_1 and L_2, respectively, the important duty ratio relationships can be expressed as follows:

$$d_2 + d_3 = \begin{cases} \frac{vin(\theta)-V_T}{L1} d_1 Ts, & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \qquad (5)$$

$$d_2 = \frac{V_B}{Vo} d_1 \qquad (6)$$

By applying charge balance of C_B over a half-line period, the bus voltage V_B can be determined. From Fig. 2.6, the average current of C_B over a switching and half-line periods are expressed as follows:

$$\langle i_{CB} \rangle_{SW} = \frac{1}{2}(i_{L1\_pk}(d_1+d_2+d_3) - I_{L2\_pkd1}) = \frac{d1^2 Ts}{2}\left(\frac{(v_{in}(\theta)-V_T)v_{in}(\theta)}{L_1 V_T} - \frac{V_B}{L_2}\right) \qquad (7)$$

And

$$\langle i_{CB} \rangle_\pi = \frac{1}{\pi}\int_0^\pi \langle i_{CB} \rangle_{sw} d\theta = \frac{d1^2 Ts}{2\pi}\left(\frac{Vpk}{L1}\left(V_{pk} V_T\left(\frac{\gamma}{2}+\frac{A}{4}\right) - B - \frac{\pi V_B}{L_2}\right)\right) \qquad (8)$$

Where the constants *A* and *B* are

$$A = \sin(2\alpha) - \sin(2\beta) \qquad (9)$$

$$B = \cos(\alpha) - \cos(\beta) \qquad (10)$$

Putting (8) to zero due to the steady-state operation, this leads to

$$V_B = \frac{MV^2 pk}{2\pi(V_B+Vo)} X\left(\pi - 2\arcsin\left(\frac{V_B+Vo}{Vpk}\right) - \frac{2(V_B+Vo)\sqrt{(Vpk+V_B+Vo)(Vpk-V_B-Vo)}}{V^2 pk}\right) \qquad (11)$$

Where M is the inductance ratio *L*2/*L*1 .

As observed from (11), the bus voltage V_B can be obtained easily by numerical method. It is noted that V_B is independent on the load, but dependent on the inductance ratio M. It is noted that the bus voltage is kept below 150 V at high-line input condition.

Similarly, the instantaneous and average input currents of the proposed circuit are

$$< i_{in} > sw = \frac{i_{L1\_pk}\, d1}{2} = \begin{cases} \frac{v_{in}(\theta)-V_T}{2L1}\, d_1^2 Ts, & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \quad (12)$$

And

$$I_{in} = \frac{1}{\pi} \int_{\alpha}^{\beta} < i_{in} > sw \, d\theta$$

$$= \frac{d1^2 Ts}{2\pi L1} [V_{pk}B - \gamma V_T] \quad (13)$$

Using (12) and (13), the rms value of the input current, average input power and power factor are given by

$$I_{in\_rms} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\beta} (< i_{in} > sw)^2 d\theta}$$

$$= \frac{d1^2 Ts}{2\sqrt{\pi} L1} \sqrt{V_{pk}^2 (\frac{\gamma}{2} + \frac{A}{4}) - 2V_{pk} V_T B + \gamma V_T^2} \quad (14)$$

$$P_{in} = \frac{1}{\pi} \int_{\alpha}^{\beta} v_{in}(\theta) < i_{in} >_{sw} d\theta$$

$$= \frac{d1^2 Ts Vpk}{2\pi L1} [\, Vpk(\frac{\gamma}{2} + \frac{A}{4}) - V_T B] \quad (15)$$

$$PF = \frac{\frac{1}{\pi}\int_{\alpha}^{\beta} v_{in}(\theta) < i_{in} >_{sw} d\theta}{\frac{Vpk}{\sqrt{2}} I_{in\_rms}}$$

$$= \frac{\frac{2}{\pi} Vpk(\frac{\gamma}{2} + \frac{A}{4}) - V_T B}{\sqrt{V^2 pk(\frac{\gamma}{2} + \frac{A}{4}) - 2V_{pk} V_T B + \gamma V_T^2}} \quad (16)$$

4.2. Condition for DCM

To ensure both cells working in DCM mode throughout the ac line period, we must determine their critical inductance first. To allow L_1 working in DCM and from (5), we have the following inequalities:

$$d_2 + d_3 \le 1 - d_{1\_PFC} \quad (17)$$

and

$$d_{1\_PFC} \le \begin{cases} \frac{V_T}{v_{in}(\theta)}, & \alpha < \theta < \beta \\ 0, & otherwise \end{cases} \quad (18)$$

where d_{1_PFC} is the maximum d_1 of the PFC cell.

For the buck–boost dc/dc cell working in DCM mode, the following inequality must be held:

$$d_2 \le 1 - d_{1\_DC/DC} \quad (19)$$

From (6) and (19), the maximum d_1 of the dc/dc cell is

$$d_{1\_DC/DC} \le \frac{V_o}{V_o + V_B} = \frac{V_o}{V_T} \quad (20)$$

Due to sharing switch in both cells of the converter, the maximum duty cycle d_{1_max} of the proposed converter is

$$d_{1\_max} = \begin{cases} \min\left(d_{1-PFC}, d_{1-\frac{DC}{DC}}\right), & \alpha < \theta < \beta \\ d_{1-DC/DC}, & \text{otherwise} \end{cases} \quad (21)$$

By applying input–output power balance of the PFC cell and substituting (21) into (15), the critical inductance L_{1_crit} is given by

$$L_{1\_crit} = \frac{R_{L-min} Ts V_{pk} V_T}{2\pi Vo^2} \left(Vpk\left(\frac{\gamma}{2} + \frac{\sin(2\alpha) - \sin(2\beta)}{4}\right) + V_T(\cos(\beta) - \cos(\alpha)) \right) d_{1-max}^2 \quad (22)$$

Where R_{L_min} is denoted as the minimum load resistance of the converter.

For the dc/dc cell sustaining all the power to the load under DCM operation in Mode A, the critical inductance L_{2_crit} is the smallest. Under the input–output power balance of the dc/dc cell, the critical inductance L_{2_crit} can be determined. The input power of the dc/dc cell in Mode A is given by

$$P_{in\_DC/DC} = \frac{V_B}{\pi} \int_{0}^{\pi} < i_{DC/DC} > sw \, d\theta = \frac{V_B^2 Ts}{2L_2} d_1^2 \quad (23)$$

Where $< i_{dc/dc} >_{sw}$ is the instantaneous input current of dc/dc cell.

Hence, by substituting (21) into (23), the critical inductance L_{2_crit} is given by

$$L_{2\_crit} = \frac{R_{L-min} V_B^2 Ts}{2V_0^2} d_{1-max}^2 \quad (24)$$

4.3. Components Stresses

Before embarking on calculating stresses on the devices, there are two characteristics of the circuit to be clarified. Interestingly, the current passing through the diode D_2 is the difference of current between i_{L2} and i_{L1} at the time interval $d_1 Ts$. Both inductor currents flows into the diode at the interval, but in opposite direction. In addition, unlike the boost-type single-stage ac/dc converter, the current of the switch S_1 is i_{L2}, but not the superposition current of both

inductors. Thus, the simultaneous currents of the diode D_2 and switch S_1 at interval d_1Ts are

$$i_{D2} = i_{L2} - i_{L1} \quad (25)$$

$$i_{S1} = i_{L2} \quad (26)$$

The rms current stresses on the diodes and switch are determined by averaging their rms current in a switching cycle over a half-line period. The rms current stress on the diode D_1 over a switching cycle is

$$I_{D1,\,sw\_rms} = \frac{Ts}{L_1}\sqrt{\frac{d_1^3(vin(\theta)-2V_T)^3}{3V_T}} \quad (27)$$

Then, by taking the average of (27) over a half-line period, its rms current stress is obtained as (28),

$$I_{D1,hf-rms} = \frac{T_s}{3V_T L_1}\sqrt{\left(\frac{d_1^3}{\pi}\left[-\gamma V_T\left(8V_T^2 + 3V_{pk}^2\right) + 3V_{pk}B\left(\frac{V_{pk}^2}{4} + 4V_T^2\right) - \frac{3V_T V_{pk}^2 A}{2} - \frac{V_{pk}^3 C}{12}\right]\right)} \quad (28)$$

where $C = \cos(3\alpha) - \cos(3\beta)$.

Similarly, the current stresses on the other semiconductor devices can be calculated easily as

$$I_{D2,\,hf\_rms} = \frac{T_s}{L_2}\sqrt{\frac{d_1^3}{3\pi}[2\alpha V_B^2 + E]} \quad (29)$$

$$I_{D3,\,hf\_rms} = \frac{V_B T_s}{L_2}\sqrt{\frac{d_1^3(V_B - Vo)^3}{3}} \quad (30)$$

$$I_{s1,\,hf\_rms} = \frac{V_B T_s}{L_2}\sqrt{\frac{d_1^3}{3}} \quad (31)$$

Where

$$E = \frac{1}{L_1^2}\left(\gamma(V_B L_T + L_2 Vo)^2 - 2L_2 V_{pk} B\,(V_B(L_1 + L_2) + L_2 Vo) + \frac{L_2^2 V_{pk}^2}{2}\left(\gamma + \frac{A}{2}\right)\right)$$

4.4. Capacitors Optimization

To determine the size of the intermediate bus capacitor C_B , we can consider the hold-up time (t_{hold_up}) of the circuit. The bus capacitor C_B will sustain all the output power within t_{hold_up} when the ac input source is removed. In normal practice, the hold-up time is one of the ac line cycle. In addition, the maximum capacitance of C_B to meet this hold-up time requirement is determined under the low-line and full output load conditions. Thus, the size of C_B is expressed as follows:

$$C_B = \frac{2Po\ t_{hold-up}}{(V_B@90V_{rms})^2} \quad (32)$$

where hold up time is:

$$t_{hold-up} = \frac{\alpha}{\omega} = \arcsin\left(\frac{V_B + V_o}{V_{pk}}\right) \quad (33)$$

Apart from the size of C_B, it is noted that the line frequency ripple on the output capacitor *Co* is inevitable since a portion of the input power is coupled to the load directly. However, this ripple can be reduced by increasing its capacitance.

4.5. DISTRIBUTION OF DIRECT POWER TRANSFER

In a conventional two-stage or S^2 PFC ac/dc converter, there are two functional cells, i.e., PFC cell and dc/dc cell. AC input power is first transferred into somewhat pulsating dc power stored on intermediate bulk capacitors by the PFC cell. The stored dc power on the bulk capacitors is processed again by the dc/dc cell to the desired dc output power. So the input power is processed twice to reach the output, as shown in Fig. 4.5(a). Direct power transfer approaches will allow a part of the input power to be processed only once and let the remaining input power to be processed twice while still achieving both high power factor and tight output regulation. Those power transfer approaches provide a new way to achieve more efficient and higher power rating PFC converters than the conventional double power processing approach. A block diagram of the proposed power transfer approach with the DPT concept is expressed in Fig. 4.5(b). In Fig. 4.5(b), portion of the power from the PFC cell is directly transferred to the output, and the remaining power from PFC cell is stored in the intermediate bus capacitor and then processed by the dc/dc cell.

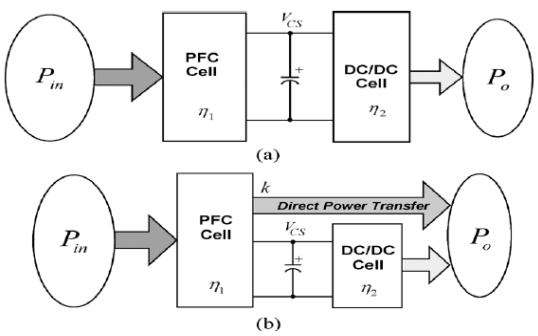


Fig. 4.5: Power Transfer Block Diagrams of PFC ac/dc Converters: (a) Conventional Power Transfer and (b) Proposed Power Transfer with DPT Concept

The interaction of power processing between both PFC and dc/dc cells under low and high-line conditions is described as

$$p_o(\theta) = p_{o\_PFC}(\theta) + p_{o\_DC/DC}(\theta) \qquad (34)$$

where $po\ (\theta)$, $p_{o\_PFC}(\theta)$, and $p_{o\_\ DC/DC}(\theta)$ are denoted as instantaneous output power of the converter, output power of PFC cell and output power of dc/dc cell, respectively. Both instantaneous output powers of PFC and dc/dc cells can be calculated as

$$p_{o\_PFC}(\theta) = \mathrm{Vo} < i_{L1}(\theta) > sw$$
$$= \begin{cases} \frac{(d_1(\theta))^2 VoT_s}{2}\left[\frac{v_{in}(\theta)(v_{in}(\theta)-V_T}{L_1 V_T}\right], & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \qquad (35)$$

$$p_{o\_DC/DC}(\theta) = p_{in\_DC/DC}(\theta) = V_B < i_{DC/DC} > sw$$
$$= \frac{V_B^2 Ts}{2L_2}(d_1(\theta))^2 \qquad (36)$$

where $p_{\mathrm{in\_dc/dc}}(\theta)$ and $d_1(\theta)$ are defined as the instantaneous value of input power of the dc/dc cell and duty cycle d_1 . From (35) and (36), it can be seen that $d_1(\theta)$ plays a crucial role in this analysis. $d_1(\theta)$ can be obtained easily once the average output current of the converter is determined. By considering the average currents of i_{L1} and i_{d3} over a switching cycle, the average output current of the converter is given by

$$Io = \begin{cases} \langle i_{L1}(\theta)\rangle sw + \langle i_{d3}(\theta)\rangle sw\ , & \alpha < \theta < \beta \\ \langle i_{d3}(\theta)\rangle sw\ , & \text{otherwise} \end{cases}$$
$$= \begin{cases} \frac{(d_1(\theta))^2 VoT_s}{2}\left[\frac{v_{in}(\theta)(v_{in}(\theta)-V_T)}{L_1 V_T} + \frac{V_B^2}{L_2 V_o}\right], & \alpha < \theta < \beta \\ \frac{(d_1(\theta))^2 T_s V_B^2}{2L_2 V_0}, & \text{otherwise} \end{cases} \qquad (37)$$

Hence, $d_1(\theta)$ in a half-line period is expressed as

$$d_1(\theta) = \begin{cases} \sqrt{\frac{2P_0}{V_o T_s\left[\frac{v_{in}(\theta)(v_{in}(\theta)-V_T)}{L_1 V_T} + \frac{V_B^2}{L_2 V_o}\right]}}, & x < 0 \\ \sqrt{\frac{2L_2 P_0}{V_B^2 T_s}}, & \text{otherwise} \end{cases} \qquad (38)$$

By substituting (38) into (35) and (36), the simultaneous output power of the converter and power distribution of the PFC and dc/dc cells are obtained.

V. DESIGN OF THE SIMULATION AND HARDWARE PROTOTYPE

The performance of the proposed circuit is verified by using MATLAB/ Simulink. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage (< 150V) and high power factor (> 96%), the inductance ratio has to be optimized. The reason for selecting 150 Vrms as a turning point is that this voltage is not a common voltage level for commercial and industrial applications even in low and high line applications. Even if 150 Vrms is a critical voltage, other voltage can also be set as a turning point. The lower the bus voltage of the converter, the lower voltage rating capacitor (150 V) can be used.

5.1. Specifications

1. Output power: 10 W
2. Output voltage: 12 Vdc
3. Power factor: > 96%;
4. Intermediate bus voltage: < 150V
5. Line input voltage: 90–270 Vrms/50 Hz
6. Switching frequency (fs): 20 kHz.

5.2. Component Specifications

Input voltage given to the circuit is 230 V and the output obtained from the circuit is 12V dc. By using equations from (1) to (38), we get the values of inductors, capacitors and resistive loads. The values used in simulation are

1. Filter inductor =1mH
2. Filter capacitance = 1μF
3. Inductor L1 = 750 μH
4. Inductor L2 = 300 μH
5. Capacitor C_0 = 2200 Mf
6. Capacitor C_B = 22μF

5.3. Simulation

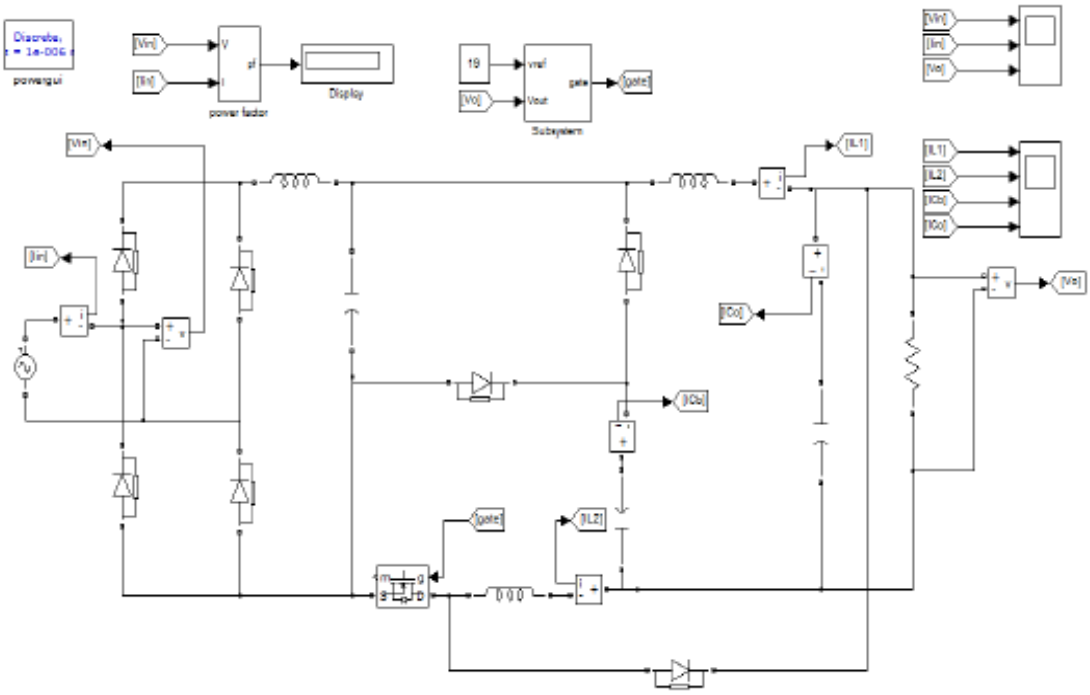
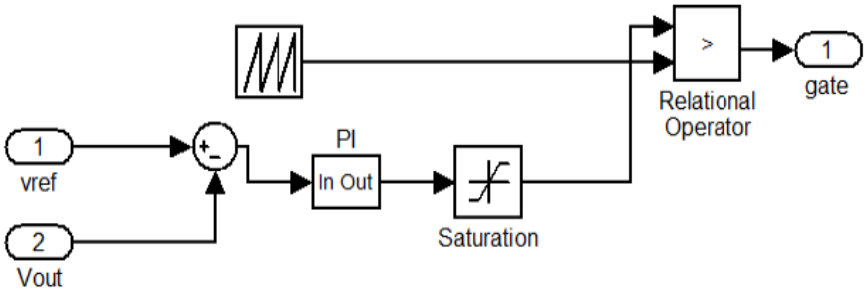


Fig. 5.1: Proposed Circuit In MATLAB/Simulink

5.3.1. Subsystem

Pulse generating system



PF measurement

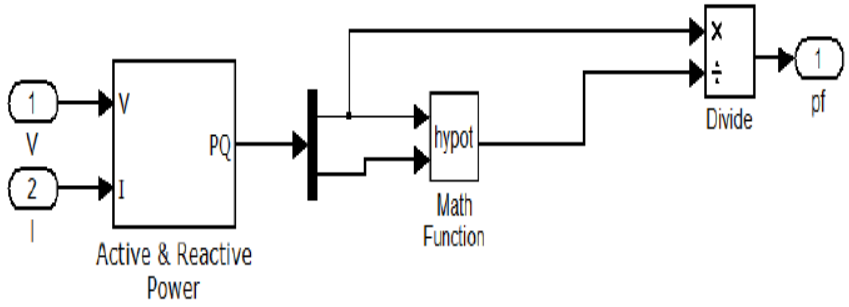


Fig. 5.2: Different Subsystems used in Simulation

5.4. Simulation Results

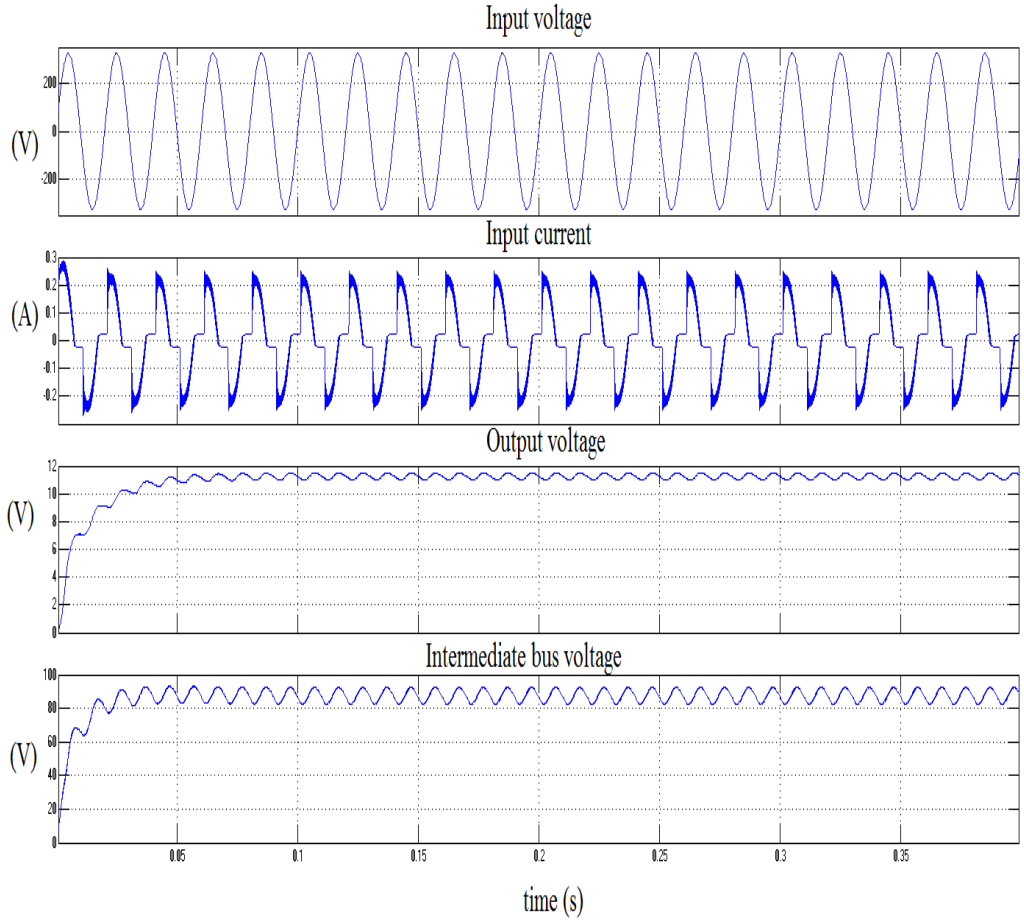


Fig. 5.3: Waveforms of Input Voltage, Input Current, Output Voltage and Intermediate Bus Voltage

The waveform of input voltage, input current, output voltage and intermediate bus voltage is shown in fig 5.3. From the waveform, for a line input voltage of 230Vrms, the output voltage is obtained as 12V and the intermediate bus voltage is 94V which is well below 150V and proved that the converter is operated in discontinuous conduction mode.

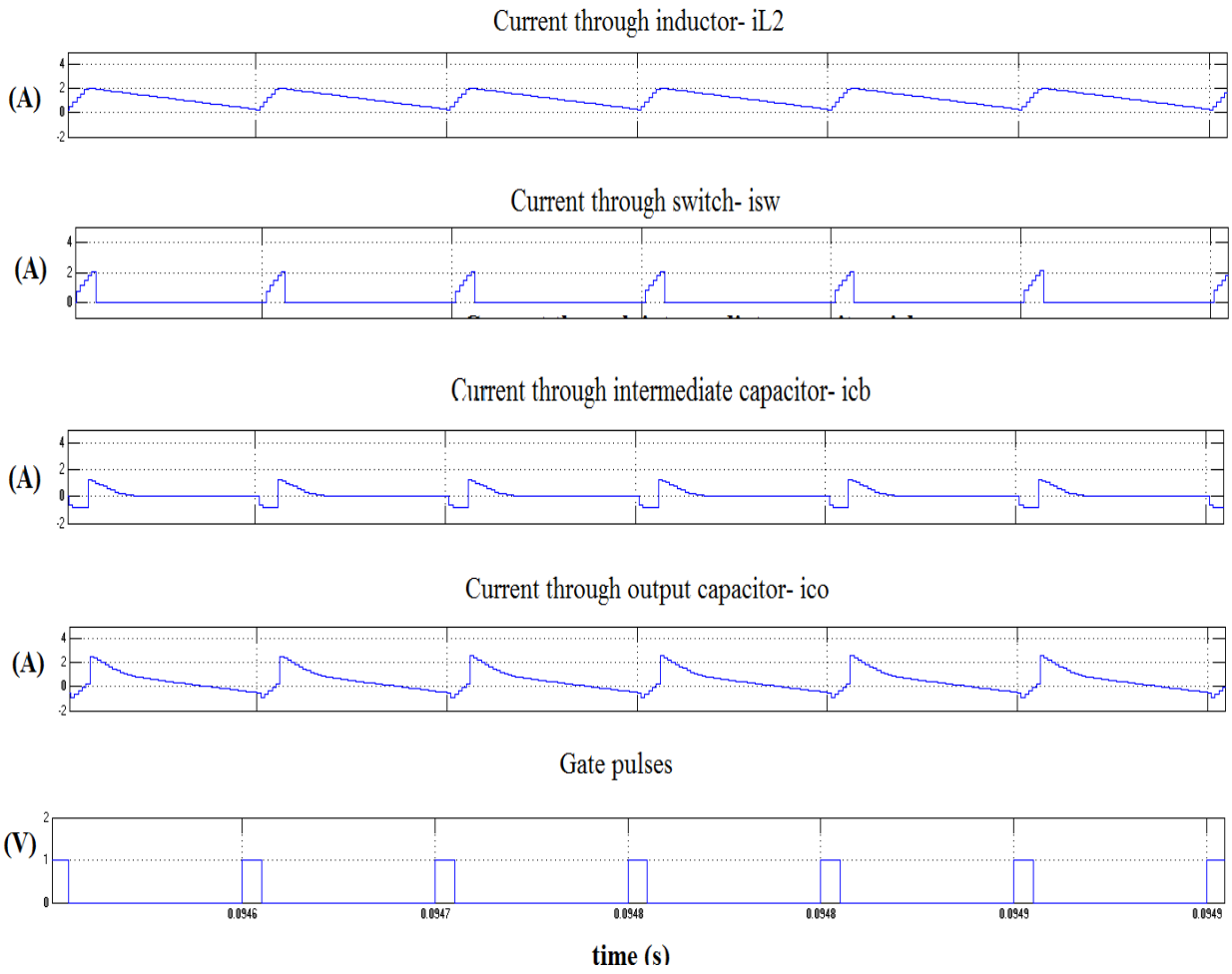


Fig. 5.4: Waveforms of iL1, iL2,isw iC_B, iC_O and Gate Pulse

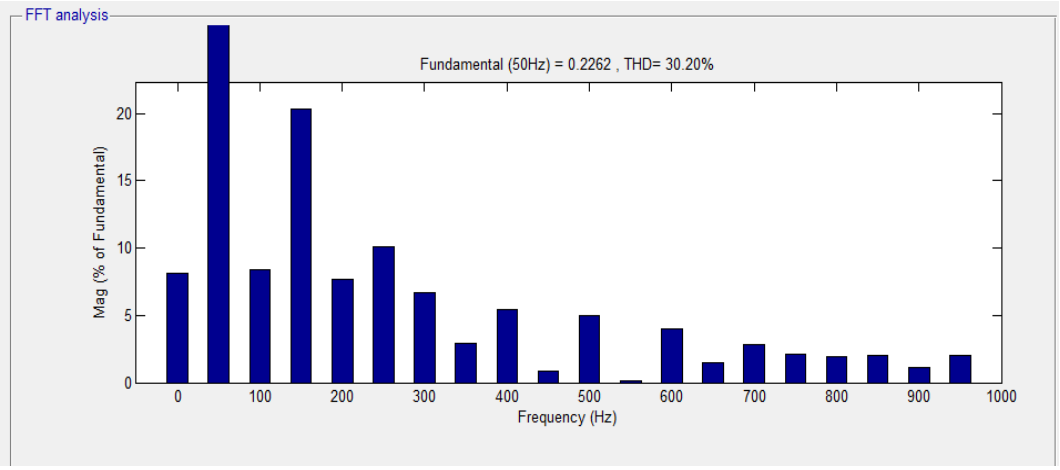


Fig. 5.5: FFT Analysis

From fig 5.5, the total harmonic distortion was obtained as 30.20%

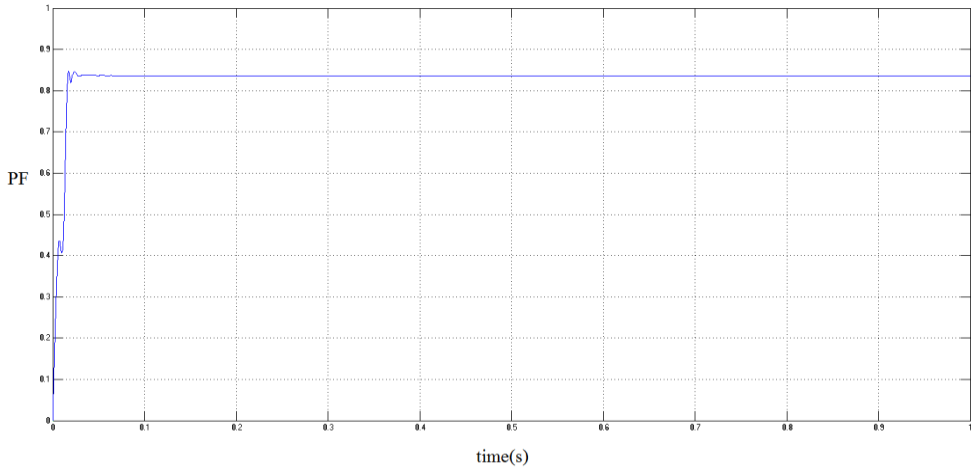


Fig 5.6.Waveform of power factor

5.5. Hardware Setup

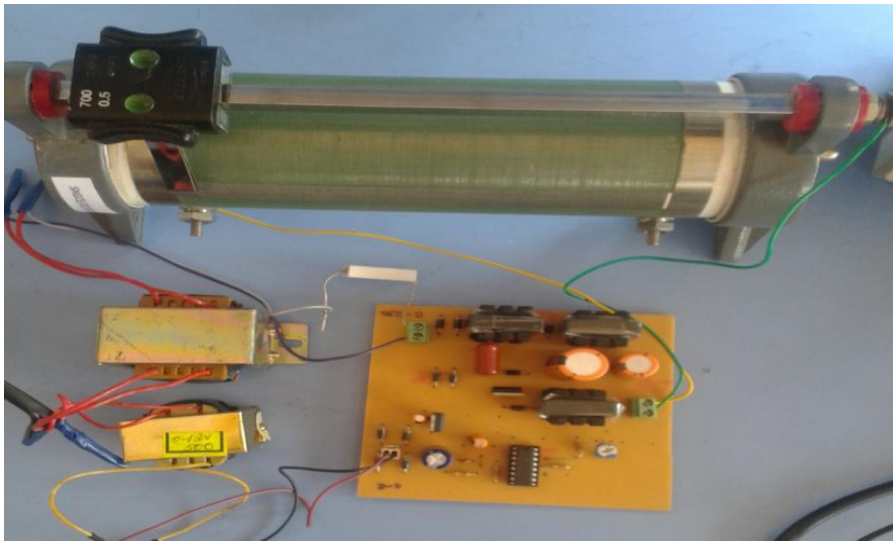


Fig. 5.7: Experimental Prototype of the Proposed Converter

5.5.1. Hardware Results

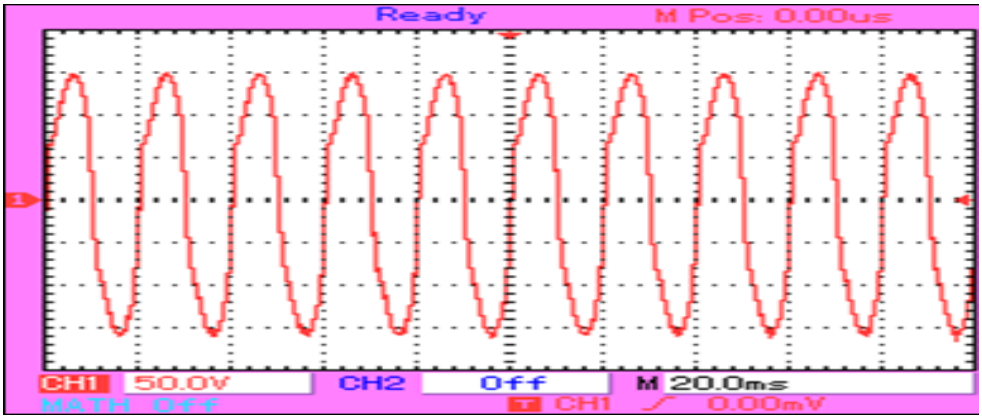


Fig. 5.8: Measured Input Voltage Waveform

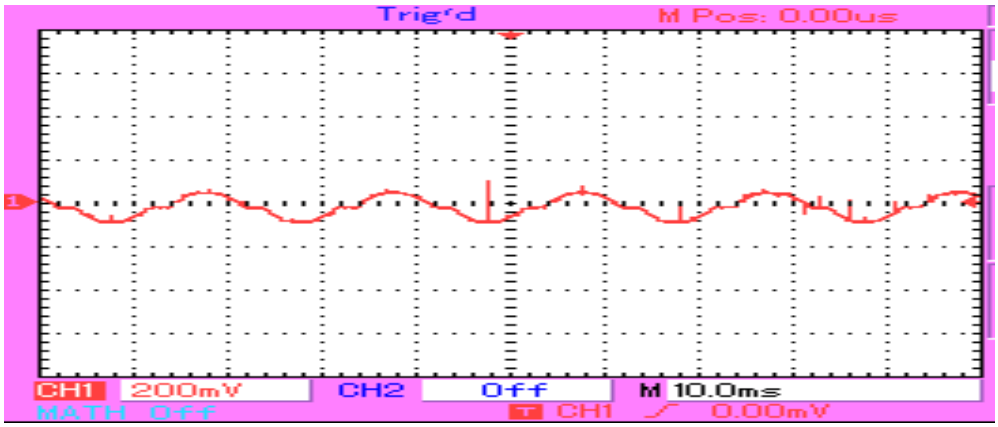


Fig. 5.9: Measured Input Current Waveform

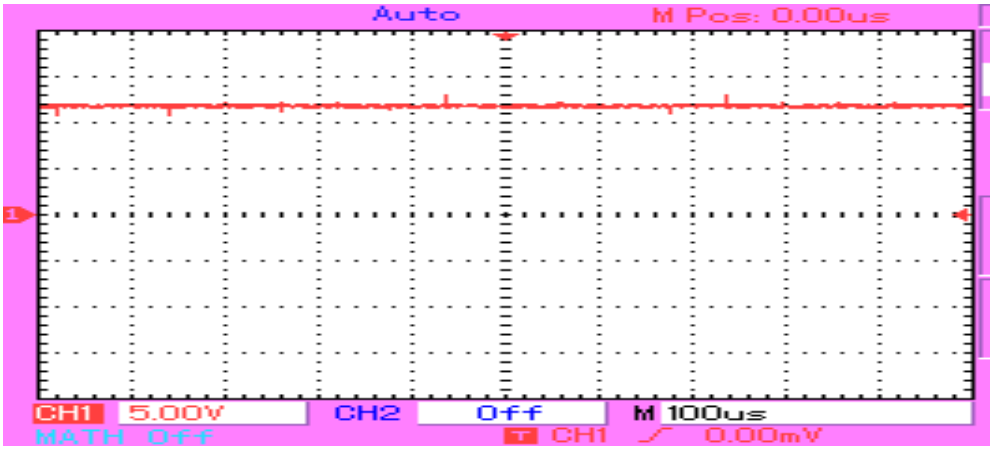


Fig. 5.10: Measured Output Voltage Waveform

After analysis it can be seen that the increase of V_B will lower the conversion efficiency of dc/dc cell due to larger voltage conversion around ten times at high-line condition, from *VB* = 94 V down to *Vo* =12 V. As a result, it further impairs the efficiency of the converter at high-line operation. On the other hand, from (7), decrease of V_B extends the conduction angle of the converter leading to higher power factor. However, lower V_B requires decrease of inductance ratio resulting in higher peak inductor currents and causing higher conduction loss. Thus, trade off has to be made for selecting the inductance ratio among the peak current of both inductors, bus voltage, and power factor. It can be seen that the proposed converter is able to achieve the lowest bus voltage at high-line condition with low output voltage and probably higher efficiency among all existing transformer-less topologies and its structure is simpler. In addition, comparing with other topologies at low-line condition, the proposed converter is also able to achieve the lowest bus voltage with positive output voltage and probably higher efficiency. Thus, the proposed converter has better performance for lower output voltage operation.

VI. CONCLUSION

The proposed AC/DC converter has been simulated, and the waveforms have been observed. The intermediate bus voltage of the circuit is able to keep low at all input and output conditions and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. Moreover, the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of transformer, the demagnetizing circuit, the associated circuit dealing with leakage inductance and the cost of the proposed circuit are reduced compared with the isolated counterparts. Because of the direct power transfer

path in the proposed converter, it is able to achieve high efficiency.

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