Timing Error Tolerance in Small Core Designs for SOC Applications

K. Sumaya Beegam and R. Dharmalingam

Abstract--- In this work, we present a low cost, multiple timing error detection and correction technique, which is based on a new flip-flop design. The proposed design methods as provides timing error tolerance at the small cost of one clock cycle delay in the circuit operation for each error correction. In addition, it is characterized by very low silicon area need are compared to previous design methods in the open literature. To validate its efficiency, it has been applied in the designs based on done. The proposed error detection and correction scheme is based on the bit-flipping flip-flop method. This is synopsized as follows: in case of error detection at the output of a flip-flop the corresponding logic value is asynchronously complemented for error correction.

I. INTRODUCTION

Due to shrinking feature sizes and increasing transistor densities, the number of processor/memory cores on a chip and their speed of operation are increasing. In future methods on chip (SoCs), transactions between the cores will become a major bottleneck for system performance as current bus-based communication architectures will be inefficient in terms of throughput, discontinuation star, and power consumption. Scaling of transistors is accompanied by a decrease in supply voltage and an increase in clock rate. This makes wires capricious as the effect of various noise sources (such as crosstalk and coupling noise) increases. With technology scaling, the wire delay as a fraction of the total delay is increasing. The delay in functioning a chip diagonally for 45-nm technology is around 6–10 cycles, with only a small fraction of chip area (0.6%–1.4%) being reachable in a single clock cycle. To effectively design future SoCs, networks on chip (NoCs), a communication-centric design paradigm to counter the delay and reliability issues of wires, has been proposed**.** Current design techniques are based on a worst case design approach that considers all the delay variations that can possibly occur due to the various noise sources and environmental effects and targets a safe operation of the system under all conditions. The system state is designed safe if there are no timing violations for all operating conditions and in the presence of the various noise sources. Such a conservative architecture approach targets timing-error-free operation of the system. In Razor, an aggressive better-than-worst-case design approach was presented for processor pipelines. In such an arrangement, the voltage margins that traditional methodologies require are eliminated, and the methodology is designed to dynamically detect and correct circuit timing errors that may occur when the worst case noise variations occur. Dynamic voltage scaling (DVS) is used along with the aggressive architecture methodology, allowing the system to operate robustly with minimum power consumption.

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II. EXISTING SYSTEM

THE CMOS technology scaling, the increase of flow variations, the susceptibility of nanometer devices to various performance degradation mechanisms, the power supply reduction and the increasing complexity of modern integrated circuits (ICs) affect their accuracy and set error rate levels outside specifications. Various mechanisms like coupling noise, power supply disturbance, jitter and temperature fluctuations are accused for timing error execution. Moreover, transistor aging mechanisms

significantly impact the performance of nanometer circuits resulting in the appearance of timing errors deliberately earlier with methods evolution during their normal lifetime. Such cases are the Negative-Positive Bias Temperature Instability (NBTI-PBTI) induced aging of PMOS-NMOS transistors respectively and the hot-carrier injection (HCI) convinced aging of NMOS transistors.

These phenomena degrade transistors' threshold voltage over time increasing path delays. Furthermore, modern systems running at multiple frequency and voltage levels (e.g. abusing dynamic voltage-frequency scaling–DVFS techniques) may present increased timing error rates due to numerous environmental and process related as well as data dependent variability's that affect circuit performance.

Path delay deviations, due to process variations, and manufacturing defects that affect circuit speed may also result in timing errors that are not easily appreciable (in terms of test cost) in high device count ICs. The inability of fabrication test procedures to exhaustively exercise the huge number of ways in nanometer circuit designs and effectively screen out all timing related defective ICs, increases the probability of test escapes. Additionally, and for the same reasons, timing authentication turns to be a hard task escalating the probability of timing failures in a design.

The Standard Scan Flip-flop

Figure 1 illustrates a pipeline stage entry frame up by acknowledged search Flip-Flops. That the Scan_EN signal is when "high" the circuit is in the operation mode of operation, for testing purposes, and the scan Flip-Flops are fed by the Scan_IN inputs. Aiming to provide the circuit with the ability of concurrent timing error detection and correction the scan Blade Flip-Flop, to be used in the register of a pipeline stage, is proposed and presented. The new Flip-Flop consists of the standard scan Flip-Flop plus a two input multiplexer (MUX) and a two input XOR gate. This extra hardware cost is very small compared to the Razor scheme where an additional shadow latch is used. The XOR gate directly compares the data at the M input and the Q output of the Main Flip-Flop for error detection, while the feedback from the M line to the input of the extra MUX forms the required memory element for error correction. The main characteristic and the advantage of the proposed topology is that we do not insert any circuitry in the critical path from the D input of the Flip-Flop to its Q output. Thus, the delay penalty is negligible and dedicated only to the small extra parasitic capacitances of the MUX input that is fed by the M line as well as this of the XOR input that is driven by the Q output.

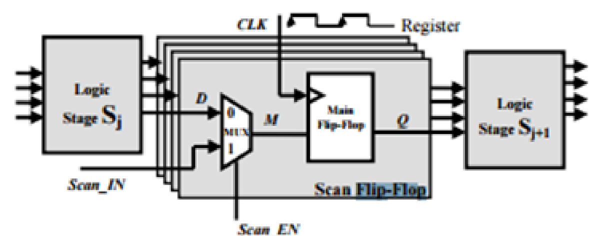


Figure 1: The Standard Scan Flip-Flop

The additional memory element that iss required in the Blade topology is constructed by the two MUXs and the feedback path from the M line, as we mentioned earlier. Its memory state is activated by the Capture signal which in the error free case is controlled by the Cap_CLK signal, a delayed version of the clock signal CLK with a lower duty cycle. An OR gate is used to provide the register error indication signal Error_Rj from the local error signals (Error) of the XOR gates in the Blade Flip-Flops of a register. Finally, the error indication signal Error_Rj is captured in a single Flip-Flop (Error Flip Flop) at the falling edge of the Cap_CLK signal. When the Cap_CLK signal is high the Capture signal is activated (turns also to high) and the MUXs latch enters the memory state; else the MUXs latch is transparent. The time interval that the Capture signal is active must coincide with the time interval where the D inputs of the Blade Flip-Flops, in all stage registers, change functions due to an earlier evaluation of the pertinent logic stages according to the circuit specifications. Any signal communication at the D inputs of the Blade

Flip-Flops, outside this time interval, is considered as violation of the timing specifications and must be detected. Obviously, the deactivation of the Capture signal (its falling edge), and thereupon of the Cap_CLK signal, must take place before the Main Flip-Flop's setup time plus the delay of the scan Flip-Flop MUX so that valid information's are present at the inputs M of the Main Flip-Flops at the triggering edge of the clock CLK.

Note that the extra silicon area cost of the OR gate at the output of a Blade register is very small, one gate per register and especially when a Domino gate is used, while the Error Flip-Flop with the OR gate at its output is a onetime cost for the whole pipeline and thus an insignificant cost.

III. Proposed System

The proposed error detection and correction methods is based on the bit-flipping flip-flop concept. This is synopsized as follows: in case of error detection at the output of a flip-flop the analogous logic value is asynchronously complemented for error correction.

Figure 2(a) illustrates the new Error Detection/ Correction Flip-Flop (EDC Flip-Flop) that is applicable to confront with timing errors. Apart from the original flip flop (Main Flip-Flop), it consists of two XOR gates and a Latch. The first XOR gate compares the D input and the F output of the Main Flip-Flop and it gives the result to the Latch. The Latch feeds the second XOR gate at the output of the Main Flip-Flop. Depending on the comparison result within a specified time interval, either the F signal of the Main Flip-Flop or its accompaniment is propagated to the output Q of the EDC Flip-Flop. The Q signal feeds the subsequent logic. Briefly, the exposed timing error detection and correction technique operates as follows. Suppose that a timing error is detected at one or more inputs of the combinational logic stage Sj+1, due to a deferred response of the previous stage Sj. Thus, the response of Sj+1 will be erroneous and must be corrected. To achieve error correction, the output of each flip-flop, at the register between the two stages, where a timing error has been catched is complemented so that valid values feed the Sj+1 logic stage. Moreover, in case that this stage is not fast enough (not a shallow stage), the appraisal time of the circuit is extended by one clock cycle to guarantee its correct computation.

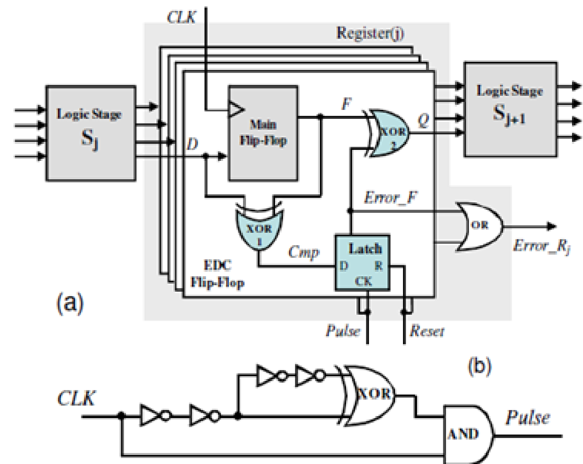
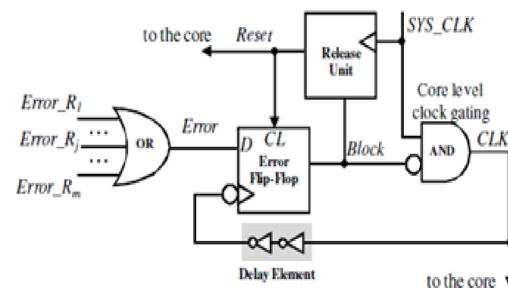


Figure 2: a) The Proposed EDC Flip-Flop and b) The Pulse Generator



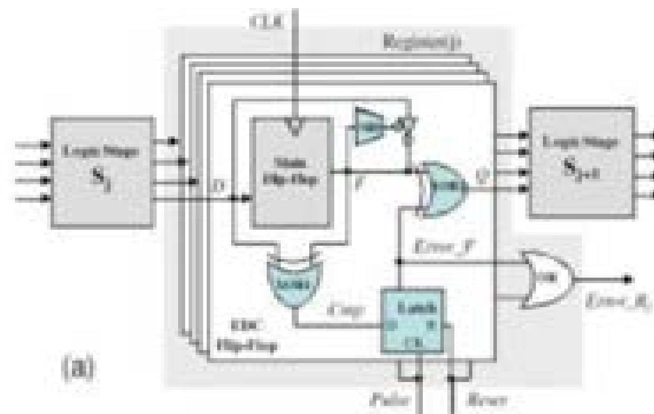
Core Level Clock Gating

The proposed EDC flip-flop is depicted in Fig, demonstrates the pulse generator used to given the clock pulse. This proposed mistake location and redress depends on the bit-flipping idea. In the event of mistake discovery in the yield of the flip–flop, comparing logical value is asynchronously complemented for error correction. The Figure 2(a) demonstrates the new Error Detection and Correction flip- flop (EDC FF) which is reasonable to timing errors. The EDC FF amount to of main flip-flop, aside from the main flip–flop, it comprises of 2 XOR gate and latch. The 1st XOR gate relates the D with F o/p of

fundamental flip-flop and result gives to the latch. The latch catches yield of 1st XOR gate and holds it. The latch bolsters the 2nd XOR gate at the yield of fundamental flip-flop. Dependent upon the comparative result of the principal XOR gate inside a pretend time interim, either F sign of principle flip-flop or the complement is basically spread to yield Q of EDC flip-flop. The Q signal feed to following resulting logical phase.

At first, the yield of the latch Error_F is made 0, since, the course of o/p of the major flip-flop F passed to the o/p of the 2nd XOR gate and then transforms to the succeeding ensuring logical phase. In the errorless scenario, the comparative results are low at the o/p of the main XOR gate on activating the clock-signal (CLK). The o/p of the primary XOR gate is arrested by the latch, in this manner the Q o/p signal gets indistinguishable to the signal F of the fundamental flip–flop that conveys exact information. This signal passes the data to the succeeding logical phases Sj+1. Nevertheless, during the timing fault in the logical phase Sj, a signal arrived lately with the aid of the fundamental flip-flop in the activating side of the clock signal. For this situation timing mistake occurring on the o/p of principle flip-flop and incorrect data is given to succeeding resulting logic phase, Sj+1. Furthermore, yield of the principle flip-flop is differs from the information signal worth D, so that first XOR gate identifies the characteristic and raises its o/p. Then a latch catches this quality and takes the response and after that 2nd XOR gate is compared with the latch o/p and the o/p of the basic flip-flop along with its o/p is Q, which is basically the complement the signal F, and this Q is passed to the succeeding resulting logic stage Sj+1, along these lines EDC FF transfers the right esteem. Importantly, the mistake is privately rectified.

A. *EDC Flip-flop with Met Stability Detector*



EDC Flip-flop with Meta-stability Detector

B. *Design of SOC with DAC*

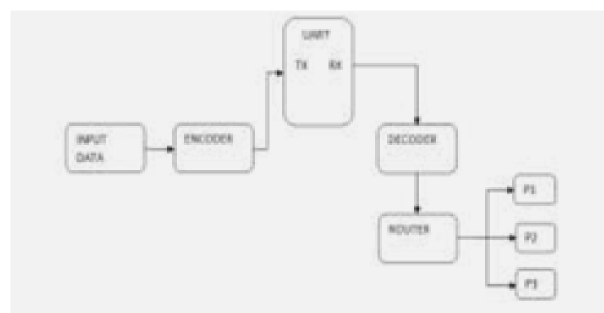


Figure 3: Block Diagram of SOC

A typical block diagram of the SoC is depicted in figure 3, the SoC intended for recognizing and remedying the error that could occur in memory unit because of radiation in lower earth circle (LEO) and owing to the stuck-at shortcomings in the memory units of space stations .The errorless information is passed to the foreordained processor utilizing serial correspondence convention. The amalgamation of error detection and correction (EDAC Unit), encoder, router and the universal asynchronous receiver and transmitter (UART) carries out the mistake recognition and remedy procedures. A block diagram of the SoC with EDAC square is depicted in figure 3; the processors are set outside of the SoC. The data is sent from beginning of space station is considered as the contribution to the encoder. Among the space related applications, the computerized information put away in the low earth circle it experiences SEU's in memory chips, these are actually prompted by radiation. Bit flips brought about by SEU's are an understood issue in memory chips and due to this the mistake is presented in framework, consequently we can utilize an error detection and correction block in the SoC for error identifying and remedying.

In case of secure transmission of data amongst the router, CPU and its neighborhood RAM, EDC flip- flop is connected during the error discovery and correction unit, hence, errors could be distinguished and revised and resultant yield will be devoid of error. In this way, the resultant error free data is passed to the processor, with the goal that it will handle the error less data and is furthermore gather every one of the information flags and deliver the resultant information yield. A timing mistake resistance strategy is introduced for enhancing the unwavering quality in flip-flop based nano-meter innovation centers. This misuses another piece flipping flip- flop that gives capacity for the identification purpose, and adjusts numerous timing errors in a circuit, with a period discipline of a solitary clock cycle. Here, the proposed methodology is described with minimal silicon area prerequisites that come with decreased complexity in design and this reduced design complexity also reduces power consumption compared to that of earlier methodologies. To enable one-cycle error correction for flip-flop based pipeline, a way to prevent the data collision in the local stalling condition should be considered. The key idea in the proposed error correction scheme is that data collisions can be avoided by gating clock signals for the master latch (m_clk) and the slave latch (s_clk) inside flip-flops independently.

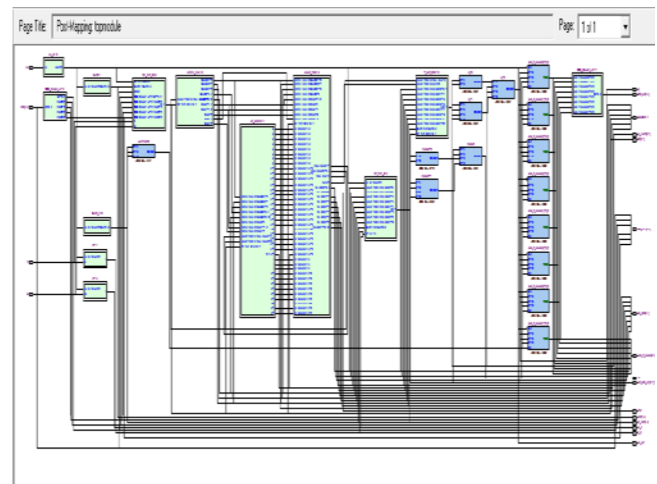
IV. Conclusion

In this work we present a new scan Flip-Flop that incorporates timing error detection/correction capabilities. In addition a pipeline architecture is discussed that exploits this scan Flip-Flop for pipeline recovery after a timing error occurrence. This approach is characterized by low silicon area requirements, negligible performance penalty and the minimum cost, of only one clock cycle, for pipeline recovery. Although the proposed technique has been illustrated for pipeline architectures, it can be applied in general to any sequential circuit. The proposed topology can be used to support architectures that exploit dynamic voltage scaling for low power operation.

In addition a The proposed circuit is characterized by low silicon area requirements, compared to earlier approaches, and negligible penalty on performance.

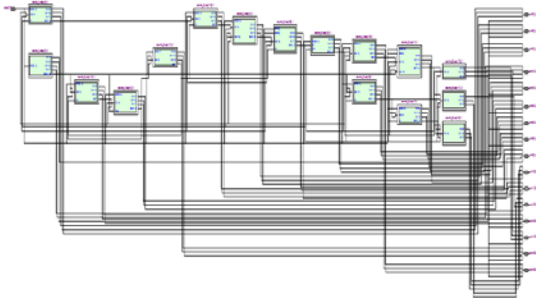
V. Results

RTL Logic for Timing Error Detection and Correction

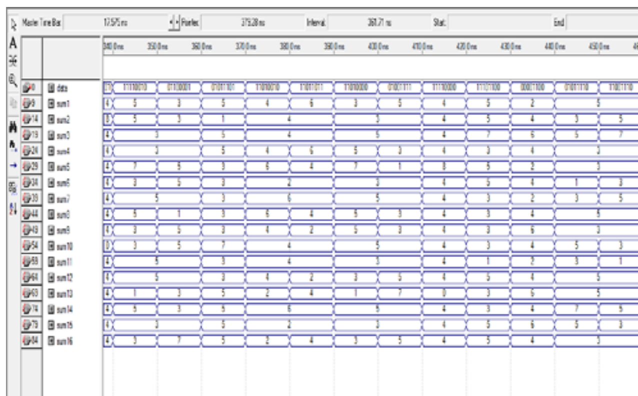


This figure shows the result of RTL schematic for the proposed Timing error detection and correction by flipping circuit

RTL Schematic for the Proposed XOR Detection

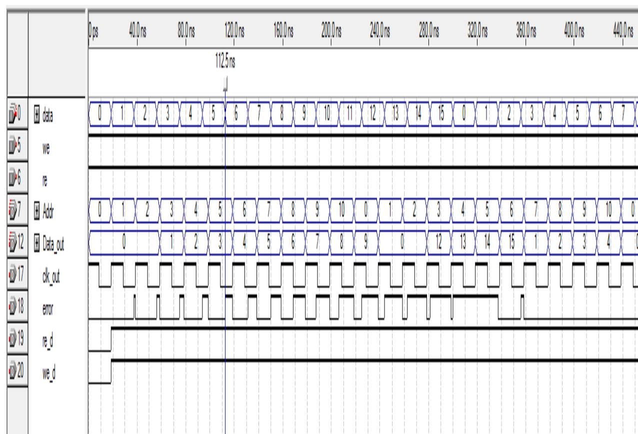


Simulation Result for XOR Detection



Here the even number of results shows the there is no error, odd number shows the error detected output. The reticular detected bit will be complemented using the flipping concept.

Simulation Result



Where the figure shows the result of timing error detection and correction.

Ports

Input Ports

Data: 4bit data input with 15 possible combinations.

Clock: 18.75ns period with 50% duty cycle.

We and re–these are the write enable and read enable port to turn on the whole circuit.

Output Ports

We_d and re_d – these are used to mention the detection is on or off? As well as correction is done or not? If those signals are high means, the detection and correction has been computed

Error shows the timing problem occurances @ the ouput

Data_out – final data out

Addr–address of the data that is @ output

REFERENCES

[1] J.W. McPherson, "Reliability Challenges for 45nm and Beyond". ACM/IEEE Design Automation Conference, Pp. 176-181, 2006.

[2] S. Mitra, N. Seifert, M. Zhang, Q. Shi and K.S. Kim, "Robust System Design with Built-In Soft-Error Resilience", IEEE Computer, Vol. 38, No. 2, Pp. 43–52, 2005.

[3] M. Agarwal, B.C. Paul, M. Zhang and S. Mitra, "Circuit Failure Prediction and its Application to Transistor Aging", IEEE VLSI Test Symposium, Pp. 277-284, 2007.

[4] M. Agarwal, V. Balakrishnan, A. Bhuyan, K. Kim, B.C. Paul, W. Wang, B. Yang, Y. Cao and S. Mitra, "Optimized Circuit Failure Prediction for Aging: Practicality and Promise", IEEE Int. Test Conference, Pp. 1-10, 2008.

[5] S.P. Park, K. Roy and K. Kang, "Reliability Implications of Bias Temperature Instability in Digital ICs", IEEE Design and Test of Computers, Vol. 23, No. 6, Pp. 8-17, 2009.

[6] T. Austin, D. Blaauw, T. Mudge and K. Flautner, "Making Typical Silicon Matter with Razor", IEEE Computer, Vol. 37, No. 3, Pp. 57–65, 2004.

[7] Y. Makris, I. Bayraktaroglou and A. Orailoglou, "Enhancing Reliability of RTL Controller-Datapath Circuits via Invariant-Based Concurrent Test", IEEE Transactions on Reliability, Vol. 53, No. 2, Pp. 269-278, 2004.

[8] M. Nicolaidis and Y. Zorian, "On-Line Testing for VLSI–A Compendium of Approaches", Journal of Electronic Testing: Theory and Applications, Vol. 12, No. 1-2, Pp. 7-20, 1998.

[9] C. Metra, R. Degiampietro, M. Favalli and B. Ricco, "Concurrent Detection and Diagnosis Scheme for Transient, Delay and Crosstalk Faults", IEEE International On-Line Testing Workshop, Pp. 66-70, 1999.

[10] M. Nicolaidis, "Time Redundancy Based Soft-Error Tolerance to Rescue Nanometer Technologies", IEEE VLSI Test Symposium, Pp. 86- 94, 1999.

[11] Y. Tsiatouhas and Th. Haniotakis, "A Zero Aliasing Built-In Self Test Technique for Delay Fault Testing", IEEE Symposium on Design for Testability of VLSI Systems, Pp. 95-100, 1999.

[12] L. Anghel and M. Nicolaidis, "Cost Reduction and Evaluation of Temporary Faults Detecting Technique", ACM/IEEE Design Automation and Test in Europe Conference, Pp. 591-598, 2000.

[13] S. Matakias, Y. Tsiatouhas, A. Arapoyanni, and Th. Haniotakis, "A Circuit for Concurrent Detection of Soft and Timing Errors in Digital CMOS ICs", Journal of Electronic Testing: Theory and Applications, Vol. 20, No. 5, Pp. 523-531, 2004.

[14] K. Kang, S.P. Park, K. Kim and K. Roy, "On-Chip Variability Sensor Using Phase-Locked Loop for detecting and Correcting Parametric Timing Failures", IEEE Transactions on VLSI Systems, Vol. 18, No. 2, Pp. 270-280, 2010.

[15] S. Valadimas Y. Tsiatouhas and A. Arapoyanni, "Timing Error Tolerance in Nanometer ICs", IEEE International On-Line Testing Symposium, Pp. 283-288, 2010.

[16] R. Samanta, G. Venkataraman, N. Shah and J. Hu, "Elastic Timing Scheme for Energy-Efficient and Robust Performance", International Symposium on Quality Electronic Design, Pp. 537-542, 2008.

[17] M. Choudhury, V. Chandra, K. Mohanram and R. Aitken, "TIMBER: Time Borrowing and Error Relaying for Online Timing Error Resilience", ACM/IEEE Design Automation and Test in Europe Conference, Pp. 1554-1559, 2010.

[18] A. Floros, Y. Tsiatouhas and X. Kavousianos, "The Time Dilation Scan Architecture for Timing Error Detection and Correction", IFIP/IEEE International Conference on Very Large Scale Integration, Pp. 569-574, 2008.

[19] S. Valadimas, A. Floros, Y. Tsiatouhas, A. Arapoyanni and X. Kavousianos, "The Time Dilation Technique for Timing Tolerance", IEEE Transactions on Computers, Vol. 65, No. 2, Pp. 654-663, 2013.

[20] D. Bull, S. Das, K. Shivashankar, G.S. Dasika, K. Flautner and D.T. Blaauw, "A Power-Efficient 32 bit ARM Processor Using Timing-Error Detection and Correction for Transient-Error Tolerance and Adaptation to PVT Variation," IEEE Journal of Solid-State Circuits, Vol. 46, No. 1, Pp. 18-31, 2011.

[21] S. Valadimas Y. Tsiatouhas and A. Arapoyanni, "Cost and Power Efficient Timing Error Tolerance in Flip-Flop Based Microprocessor Cores", IEEE European Test Symposium, Pp. 8-13, 2012.

[22] M. Omana, D. Rossi, N. Bosio and C. Metra, "Low Cost NBTI Degradation Detection and Masking Approaches", IEEE Transactions on Computers, Vol. 62, No. 3, Pp. 496-509, 2013.

[23] M. Nicolaidis, "GRAAL: A New Fault Tolerant Design Paradigm for Mitigating the Flaws of Deep Nanometric Technologies", IEEE International Test Conference, Pp. 1-10, 2007.

[24] H. Yu, M. Nicolaidis, L. Anghel and N-E. Zergainoh, "Efficient Fault Detection Architecture Design of Latch-based Low Power DSP/MCU Processor," IEEE European Test Symposium, Pp. 177-183, 2011.

[25] S. Das, C. Tokunaga, S. Pant, W.H. Ma, S. Kalaiselvan, K. Lai, D.M. Bull and D.T. Blaauw, "Razor II: In Situ Error Detection and Correction for PVT and SER Tolerance", IEEE Journal of Solid-State Circuits, Vol. 44, No. 1, Pp. 32-48, 2009.

[26] K. Bowman, J.W. Tschanz, N-S. Kim, J.C. Lee, C.B. Wilkerson, S-L. Lu, T. Karnik and V.K De, "Energy-Efficient and Metastability-Immune Resilient Circuits for Dynamic Variation Tolerance", IEEE Journal of Solid-State Circuits, Vol. 44, No. 1, Pp. 49-63, 2009.

[27] K. Bowman, J.W. Tschanz, SL. Lu, P.A. Aseron, M.M Khellah, A. Raychowdhury, B.M. Geuskens, C. Tokunaga, C.B. Wilkerson, T. Karnik and V.K De, "A 45nm Resilient Microprocessor Core for Dynamic Variation Tolerance", IEEE Journal of Solid-State Circuits, Vol.46, No. 1, Pp. 194-208, 2011.