High Performance Input Output Block Implementation on FPFA-An Overview

T. Prathibha and Dr.B. Mohankumar Naik

Abstract--- In this paper of high performance input output blocks, the study and analyze high performance digitally controlled impedance IO standards design in terms of power consumption. The digitally controlled impedance calibration circuit has high accuracy in 7 series FPGA and supports all IO standards. The IO standards which support the controlled impedance drivers such as LVDCI_15, LVDCI_18, HSLVDCI_15, HSLVDCI_18, HSUL_12_ DCI, and DIFF_ HSUL_12_DCI are designed. The low power consumption methodologies for these IO standards are studied. Xilinx planhead and xPower analyzer is used to simulate, synthesize and implement low power design.

Keywords--- IO Standards, FPGA, Low Power, LVDCI_15, LVDCI_18, HSLVDCI_15, HSLVDCI_18, HSUL_12_ DCI,DIFF_HSUL_12_DCI

I. INTRODUCTION

As field programmable gate array (FPGA) speed getting faster and bigger, PC board design became difficult and maintain signal integrity become critical issue. PC board trace must be properly terminated to avoid reflections. To address these issues and for impedance matching Xilinx developed digitally controlled impedance technology in 7 series FPGA. DCI can either control the output impedance of driver or add a parallel termination of the receiver or transmitter. DCI adjust the impedance inside the IO to calibrate to external precision reference resistors placed on VRN and VRP pins.The N reference pin (VRN)is pulled up to V_{CCO} by a reference resistor and P reference pin (VRP) is pulled to ground by another reference resistor. The value of each reference resistor is either equal to twice the characteristic impedance of the PC board trace. DCI supports only high performance IOBs.High performance (HP) IOB is designed to meet the performance requirements of high speed memory and chip to chip interface with voltage1.8v.

Basic IO Structure and IO Related Blocks

The physical structure and provide a range of IO standards, termination and power saving features. Each IO bank consists of 50 IOB. The number of banks depends on device size and package pin out.

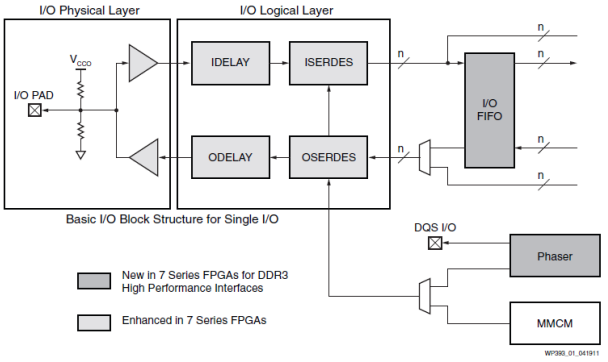

Fig. 1: 7series Basic IO Block and its Connectivity

Figure.1 shows the detailed I/O bound logic functions such as input output delays, serialization and deserialization functions, clock management, and FIFO interface features. At physical levels I/O s are required to support a range of drive voltages and drive strength and receive capabilities to interface various I/O standards. At logic levels inputs and outputs are configured as either combinatorial or registered.

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Single Ended HP IOB

The IO pins can be configured to various IO standards

- Single ended IO standards
- Differential IO standards

Each IOB contains 50 IO pins, the two pins are single ended and remaining 48 pins are differential ended standards.

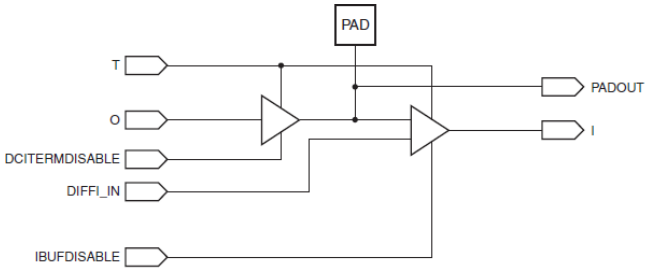

Fig. 2: Single Ended HP IOB Diagram

Figure.2 shows single ended HP IOB and its connections to the internal logic and device pad. IBUFDISABLE is input buffer primitive with disable port with additional power saving features. Differential termination supports the differential IO standards used as inputs.

II. LITERATURE REVIEW

In low power FPGA application based design, researcher deals with energy efficient IO standards LVCMOS, HSLVDCI, HSTL; LVDCI_DV2 is used to match the impedance transmission line to avoid reflections. Comparison is made among IO standards in terms of power [1]. The digitally controlled IO standards in memory interface reduce the dynamic power consumption at 1.5 and 1.8 output driver voltage comparison to 2.5 voltages [2]. Power reduction is done for different frequencies at 1GHz, 10GHz, 100GHz and 1THz and power required at 1THz is 36.09 53.14% power [3]. 50% signal power, 92% of clock power, 32-46% of IO power and 25-27% of total power is reduced when the DCI IO standards are used for ROM design [4]. IO standards are analyzed at different temperature from 45 to 70 degree Celsius with 28nm technology to implement on vertex-6 FPGA [5]. Green image ALU is designed to achieve energy efficiency for 40nm technology with the reduction of 65.67% of IO power [6].

III. DIGITALLY CONTROLLED IO STANDARDS

7 series FPGA support digitally controlled impedance IO standards like LVDCI, HSLVDCI, HSTL, differential HSTL and SSTL.

Low Voltage Digitally Controlled Impedance

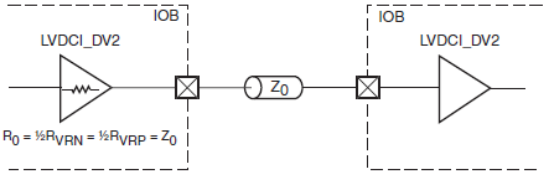

Fig. 3: Unidirectional Half Impedance LVDCI

Figuer.3 shows IO buffer configure the outputs as controlled impedance drivers. The impedance is set by the common external reference resistor with resistance equal to $Z_{0.}$

High Speed Low Voltage DCI

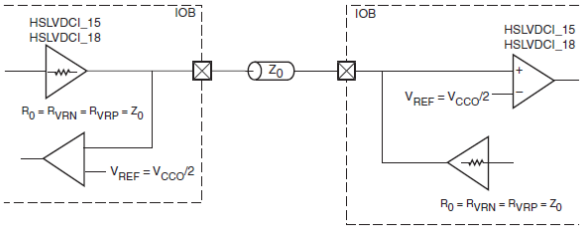

Fig. 4: HSLVDCI Controlled Impedance Driver

Figure 4 shows HSLVDCI with bidirectional termination, by using V_{REF} input it allows greater input sensitivity at the receiver side.

High Speed Transrecevier Logic

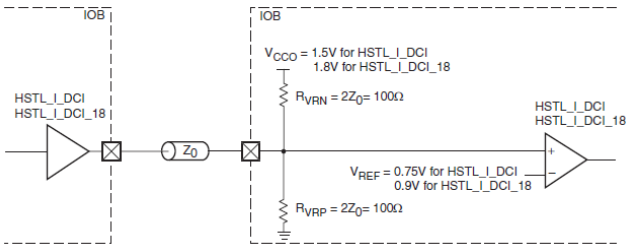

Fig. 5: HSTL Class (1.2v,1.5v or 1.8v) Termination

Figure 5 shows HSTL standard, is a general purpose high speed bus standard defined by JEDEC. It supports clocking high speed memory interface. Different versions are available which requires differential amplifier input buffer and push pull out put buffer.

Stub Series Termination Logic

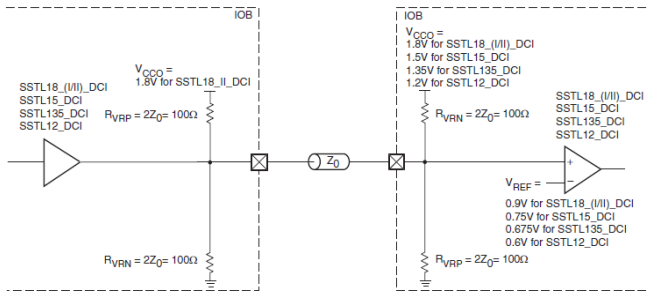

Fig. 6: SSTL Unidirectional Termination

Figure 6 shows stub series termination logic for 1.8v, 1.5v, 1.35v for general purpose memory buses. Use on-die termination at the memory device on bidirectional signals and external parallel termination resistor to V_{TT}=V_{CCO}/2 for the unidirectional signals.

IV. POWER REDUCTION METHODOLOGY

Low power design with high performance is a major issue for the designers. Power can be reduced by lowering supply rails, simplifying design, thermal management and power distribution plans. Some of the methods to reduce IO power are discussed below

- use low V_{CCAUX} – minimizes static and dynamic power
- avoid usage of internally referenced input standards
- use lowest slew/output drive/ voltage levels
- No termination or series termination are preferred over parallel termination
- Evaluate using lower voltage swing differential standards

Reducing Static Power

Supply source V_{CCINT} and V_{CCAUX} are sensitive to power, voltage and thermal variations. V_{CCAUX} supply power to input buffer and V_{CCINT} supply power to the IO with device core logic should have minimum value. Use minimum number of clock generation modules.

Reducing Dynamic Power

Dynamic power is

$$\Sigma\ \alpha,\ f_{clk,}\ C_{L,}\ V^2$$

- Activity(α, f_{clk}):depend on the input data captured and clock enable signal.
- Capacitance (C_L): depend on design constraints.
- Voltage (V^2): depend on voltage regulator and other components attached to the rails.

V. CONCLUSION

The digitally controlled impedance calibration circuit has high accuracy in 7 series FPGA and supports all IO standards.The IO standards which support the controlled impedance drivers such as LVDCI_15, LVDCI_18, HSLVDCI_15, HSLVDCI_18, HSUL_12_DCI, and DIFF_HSUL_12_DCI. The low power techniques are utilized to reduce the power reduction in IO standards implementation and comparison can be done further.

VI. FUTURE SCOPE

The high performance IO standards are designed implemented in future work on vertex-7 FPGA and the power analysis is carried out for the IO standards. Comparison of all IO standards will be carried out in terms of power.

REFERENCE

[1] Ravender kaur, jagadesh kumar, sumitha nagah, bishwajeet pandey, kavitha goswami," IO standard based low power memory design and implimentation on FPGA," 2nd international conference on computing for sustainable globa developemt(INDIAcom), 978-9-3805-4416-8/15@ 2015 IEEE.

[2] Bishwajeet pandey, ravikanth kumar," low voltage DCI based low power VLSI cicuit implementation on FPGA," IEEE conference on information and communication technologies, 978-1-4673-5758-6/13.

[3] Bishwajeet pandey, pooja saigal, ektha walia, " Design of frame buffer for 1THz energy efficient digital image processor based on HSLVDCI I/O standard in FPGA," 978-1 -4799-1 607-8/1 3/©201 3 I E E E.

[4] Rishita saini, neha bansal, meenakshi bansal, " low power high performance ROM design on FPGA using LVDCI IO standard," 6th international conference on computational intelligence and communication networks.

[5] Shivani madhok, Amanpreet kaur, Bishwajeet pandey," Different IO standard based energy effiecint decoder design for 64-bit processor architecturer," ," 2nd international conference on computing for sustainable globa developemt(INDIAcom), 978-9-3805-4416-8/15.

[6] Tanesh kumar, Bishwajeet pandey,teerath das," digitally controlled impedence based green design on ultra scale FPGA," international conference on green computing, communication and conservation of energy, 978-1-4673-6126-2/13.

[7] Ravinder kaur,Bishwajeet pandey, jagadish kumar," IO standard based low power memory design and implimentation on FPGA," 2nd international conference on computing and global development.

[8] http://www.xilinx.com/support/documentation/user_guides/ug471_7Series_SelectIO.pdf.

[9] http://www.xilinx.com/support/documentation/user_guides/ I/Oand memory interface features and benefits in 7 series architecturer.pdf.